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(54) **PIN DIODES FOR PHOTODETECTION AND HIGH-SPEED, HIGH-RESOLUTION IMAGE SENSING**

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See application file for complete search history.

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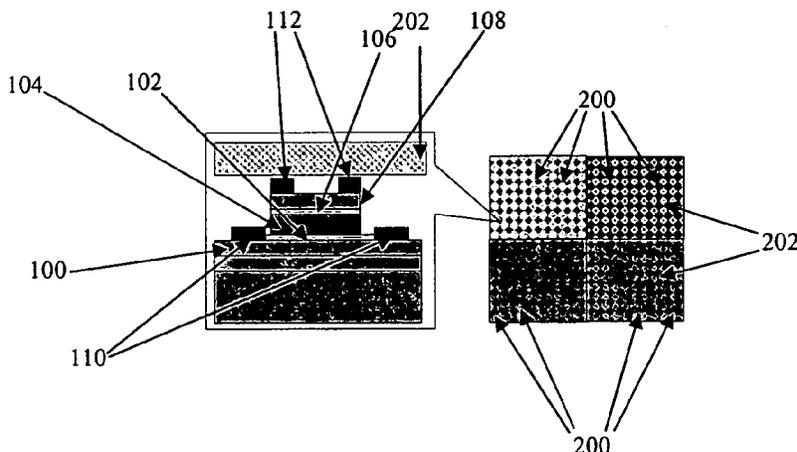
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(57) **ABSTRACT**

The present invention provides high-speed, high-efficiency PIN diodes for use in photodetector and CMOS imagers. The PIN diodes include a layer of intrinsic semiconducting material, such as intrinsic Ge or intrinsic GeSi, disposed between two tunneling barrier layers of silicon oxide. The two tunneling barrier layers are themselves disposed between a layer of n-type silicon and a layer of p-type silicon.

38 Claims, 2 Drawing Sheets



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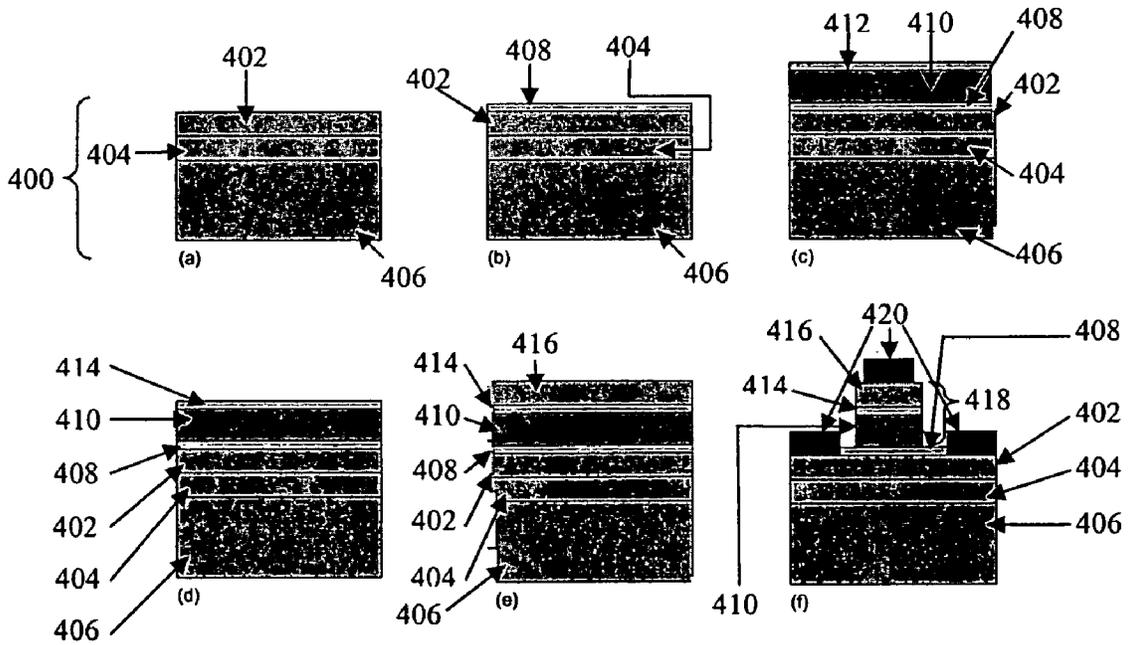
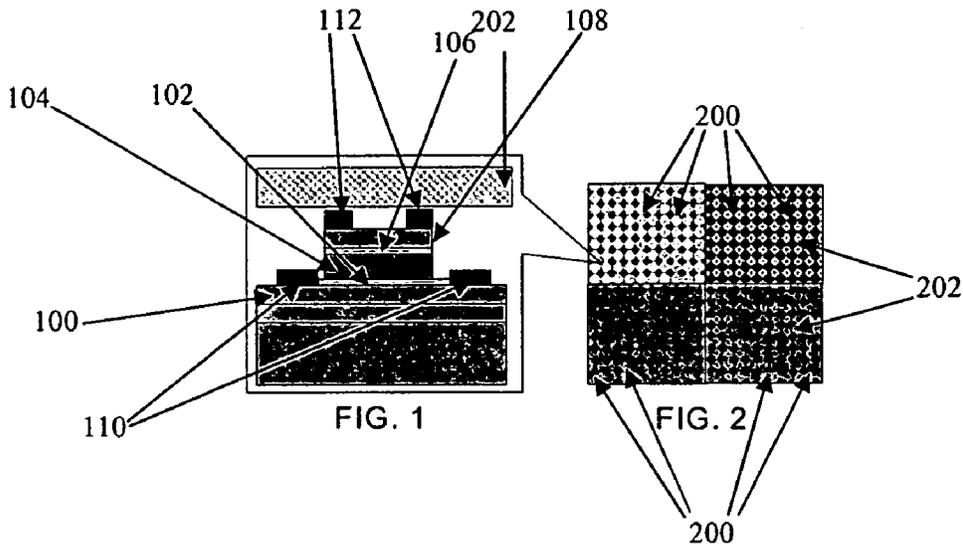


FIG. 4

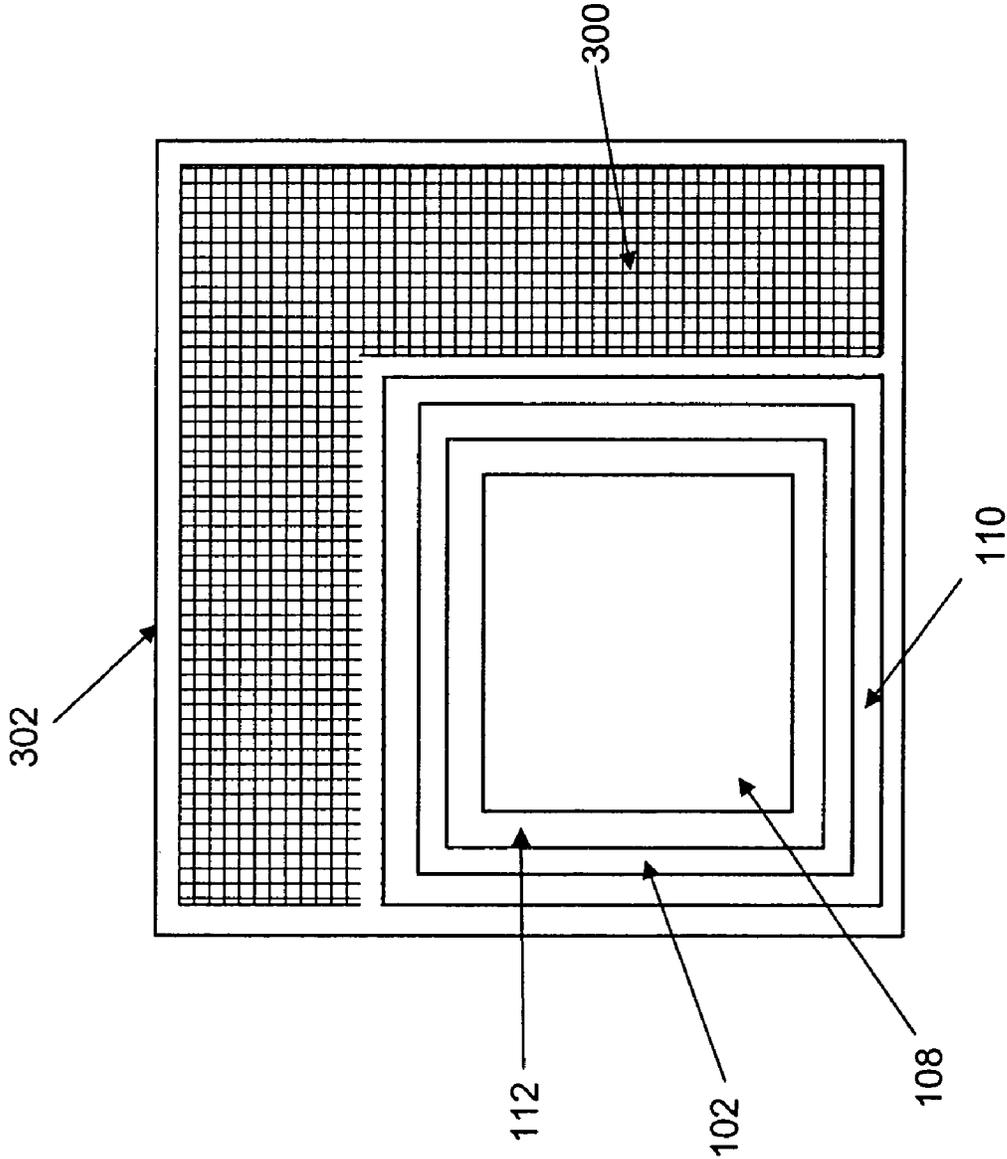


FIG. 3

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PIN DIODES FOR PHOTODETECTION AND HIGH-SPEED, HIGH-RESOLUTION IMAGE SENSING

STATEMENT OF GOVERNMENT RIGHTS

Research funding was provided for this invention by the National Science Foundation under Grant No. 0079983. The United States government has certain rights in this invention.

FIELD OF THE INVENTION

This invention relates to PIN diodes for use in photodetectors and CMOS optical imagers.

BACKGROUND

Multispectral photon detection (covering the visible and infrared) allows target identification with enhanced information content. For example, in military applications, multispectral-photodetector arrays can be used to identify real missile heads from fake ones and can help direct the antimissile head toward an actual target. The principle of multispectral detection has been widely used in astronomic observations. One available photodetection mechanism is electron-hole generation in a reverse-biased PIN diode

For PIN diode-based photodetectors, the longest wavelength that can be detected is dictated by the bandgap of the intrinsic semiconductor used for the intrinsic layer. Photons with energy higher than the bandgap energy will be detected, as long as the intrinsic layer is sufficiently thick to absorb the photons. The photodetectors must provide high efficiency and high-speed operation in order to use them for high-speed object detection. To integrate photodetectors on a CMOS chip, where high speed and sophisticated digital signal processing circuitry can be made, Group IV-based detectors may be desirable. The current approaches of making photodetectors on a Si chip generally employ thick Si PIN diodes that are vertically buried deep in the Si substrate. For these PIN diode photodetectors, efficiency can be kept high as long as the intrinsic layer is thick enough. However, the speed of these PIN diodes is rather low, because of the long tail of collection of photon current (due to the low drift velocity of holes).

Ge is a promising material for light detection in optical communication for at least two reasons. First, because of its direct bandgap at 0.8 eV and indirect bandgap of 0.66 eV, it is highly absorbing over a wide range. Second, because of its compatibility with existing Si technology, it offers the potential for high-quality CMOS compatible integrated photoreceivers. Unfortunately, due to the large lattice mismatch between Si and Ge, progress toward the formation of Ge-based high-speed photodetectors on Si has been very limited.

Some work has been done to fabricate photodetectors using growth of Ge quantum dots on Si surfaces to make many alternating layers of Si film and Ge quantum dots. Although such photodetectors provide some increase in absorption, they show only a slight improvement over Si PIN diodes.

SUMMARY OF THE INVENTION

The present invention provides high-speed, high-efficiency PIN diodes for use as photodetector, and in CMOS imagers. The PIN diodes include a layer of intrinsic semiconducting material disposed between two tunneling barrier layers of silicon oxide. The two tunneling barrier layers are themselves disposed between a layer of n-type silicon and a layer of p-type silicon.

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In a preferred embodiment, the intrinsic semiconducting material is a single-crystal germanium (Ge) nanomembrane or GeSi alloy nanomembrane and the p- and n-type silicon (Si) layers are single-crystal Si nanomembranes. The Ge or GeSi nanomembranes desirably have a thickness of no more than about 2,000 nm (the thickness depends on the tradeoff between speed and efficiency of photodetectors) and are separated by silicon oxide layers desirably having a thickness of no more than about 10 nm to provide a nanomembrane stack.

The nanomembrane stacks may be made by transferring the thin intrinsic Ge or GeSi layer onto a thin silicon layer having a very thin oxide layer on its surface. A second thin silicon layer (having a different doping type than the first) with a thin oxide layer on its surface may then be transferred onto the single-crystal Ge or GeSi layer. Alternatively, the second oxide layer may be formed on the Ge or GeSi layer by growing and oxidizing a thin layer of Si prior to the transfer of a second thin silicon layer onto the stack. In one embodiment, the Ge nanomembrane is the top device layer of a Ge-on-insulator substrate which has been released by etching away an underlying sacrificial layer (e.g., a buried oxide layer). In another embodiment, some amount of Si can be incorporated into a Ge device layer of a Ge-on-insulator substrate to form a GeSi alloy layer, which is subsequently released by etching away the underlying sacrificial layer. The released intrinsic GeSi or Ge nanomembrane may be transferred directly onto the oxidized device layer of a Si-on-insulator substrate. Alternatively, the released nanomembrane may be lifted and transferred using a host substrate.

A voltage source connected to electrodes that are electrically coupled to the n- and p-type silicon layers may be used to provide a reverse bias across the PIN diode, allowing the PIN diode to act as a photodetector. A plurality of such photodetectors may be arranged in an array to provide a photodetector array. A CMOS circuit coupled to the photodetector array may be used to provide a CMOS image sensor.

Further objects, features and advantages of the invention will be apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a wavelength-specific photodetector in accordance with the present invention.

FIG. 2 is an illustrative layout for a multispectral photodetector array in accordance with the present invention.

FIG. 3 is a schematic diagram showing a top view of the photodetector of FIG. 1.

FIG. 4 is a schematic diagram showing a method for making a photodetector in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides PIN diodes with structures that improve both the speed and efficiency of photodetectors that incorporate the PIN diodes. Photodetectors made from the PIN diodes can be easily integrated with silicon processing techniques and CMOS-based devices, such as digital imagers.

As illustrated in FIG. 1, the PIN diodes include an n-type silicon layer **100**; a first tunneling barrier layer **102** comprising silicon oxide disposed above the n-type silicon layer; a layer of intrinsic semiconducting material **104** disposed above the first tunneling barrier layer; a second tunneling barrier layer **106** comprising silicon oxide disposed above the layer of intrinsic semiconducting material; and a p-type silicon layer **108** disposed above the second tunneling barrier

layer. In a typical embodiment, each of the aforementioned layers is disposed above and in direct contact with its preceding layer.

The PIN diodes may also include a first electrode **110** electrically coupled to the n-type silicon layer and a second electrode **112** electrically coupled to the p-type silicon layer. When a voltage source is connected to the first and second electrodes and a reverse bias is applied across the PIN diode, the PIN diode acts as a photodetector, wherein photons absorbed in the intrinsic layer generate charge carriers (i.e., electrons and holes) that are collected at their respective electrodes to generate a photocurrent. When charge carriers are created in the intrinsic layer by photons of different energies, these charge carriers will also have a range of energies. The silicon oxide tunneling barrier layers have a conduction band energy that is higher than the conduction band energy of the intrinsic semiconductor material and valance band energy that is lower than the valence band energy of the intrinsic semiconductor material. Energy barriers will be present for the charge carriers. However, the thickness of the silicon oxide on both sides is very thin. Based on quantum physics, the wave function of charge carriers with sufficient kinetic energy will overlap with the thin energy barriers. Due to the overlapping of the wave function, charge carriers can be found on the other side of the oxide energy barrier. This phenomenon is well known as tunneling. Higher-energy carriers will have higher probability across the thin energy barriers. Therefore, the tunneling barrier layers allow only those electrons and holes with sufficiently high energy to tunnel through the barrier and be collected by the electrodes. By selecting those carriers having higher energies (the tunneling barriers act like an high-energy-pass filter for charge carriers), the use of tunneling barrier layers improves the speed of the photodetectors.

While the speed of the photodetectors is improved with the introduction of the tunneling barrier layers, the photocurrent collection efficiency will inevitably be sacrificed, as only the "fast" electrons and holes will be collected. For this reason, a Ge or GeSi intrinsic layer is advantageous because it increases (typically, by several orders, relative to silicon) the absorption efficiency of photons, improving the efficiency of photocurrent generation, and therefore the sensitivity of the photodetector. Ge is known to have a much higher efficiency for absorbing photons, over a wider range of wavelengths than Si. The intrinsic semiconducting material desirably comprises intrinsic Ge, desirably in the form of a thin, continuous, single-crystal nanomembrane.

In a preferred embodiment, the intrinsic layer has a thickness of no more than about 2000 nm. This includes embodiments where the intrinsic layer has a thickness of no more than about 1000 nm, further includes embodiments where the intrinsic layer has a thickness of no more than about 500 nm and still further includes embodiments where the intrinsic layer has a thickness of no more than about 200 nm. The n- and p-type silicon layers are also desirably quite thin. In some embodiments the silicon layers have a thickness of no more than about 1000 nm. This includes embodiments where the silicon layers have a thickness of no more than about 500 nm and further includes embodiments where the silicon layers have a thickness of no more than about 200 nm. The silicon oxide layers separating the n- and p-type silicon layers from the intrinsic layer typically have a thickness of no more than about 10 nm. This includes embodiments where the silicon oxide layers have a thickness of no more than about 5 nm and further includes embodiments where the silicon oxide layers have a thickness of no more than about 2 nm.

As illustrated in FIG. 2, a plurality of the photodetectors **200** may be arranged in an array to provide a photodetector array and CMOS circuitry may be coupled to the photodetector array to provide a CMOS image sensor. To achieve multispectral detection, one or more filters **202** for different wavelengths may be disposed over one or more different areas of a photodetector array. However, the use of filters is optional. These filters are widely available and can be easily implemented in the proposed photodetector arrays. The digital imaging information obtained from different areas may be processed together using CMOS digital circuitry. The CMOS circuit for image processing may be fabricated on a substrate (e.g., a silicon substrate) underlying the PIN diodes or on the n- and p-type Si layers. Photodetector arrays composed of PIN diodes and CMOS circuits for use with photodetector arrays are known. Descriptions of appropriate layouts for arrays of PIN diodes and CMOS circuits for use with arrays of PIN diodes are described in U.S. Pat. Nos. 6,809,358 and 6,831,263; the entire disclosures of which are incorporated herein by reference.

FIG. 3 shows a top view of a single pixel in a CMOS image sensor that includes the PIN diode of FIG. 1 and CMOS circuitry **300**. In the embodiment of FIG. 3, a layer of insulation **302** is disposed around the pin diode and the perimeter of the pixel.

FIG. 4 shows an example of a fabrication process flow that may be used to make high-speed and high-efficiency CMOS compatible photodetectors in accordance with the present invention. In this illustrative process, Si and Ge nanomembranes are employed. The base substrate upon which the PIN diode is fabricated is a Si-on-insulator substrate **400** that includes a thin, n-type silicon layer **402** over a buried oxide layer **404** that is supported on a silicon handle layer **406**. (See step (a).) Silicon layer **402** has a thin oxide layer **408** on its surface. (See step (b).) Oxide layer **408** may be a native oxide layer or may be generated by a separate oxidation process. Silicon layer **402** does not have to be the template layer of a silicon-on-insulator wafer, as in FIG. 4. Instead, silicon layer **402** and its oxide layer **408** may be pre-fabricated and transferred from a separate substrate. A single-crystal intrinsic Ge layer **410**, which has been released from a Ge-on-insulator substrate by removing a sacrificial layer under the Ge layer, is transferred and bonded to silicon oxide layer **408**. Ge layer **410** may be transferred with a pre-grown Si layer **412** which is subsequently oxidized to provide a silicon oxide layer **414**. (See steps (c) and (d).) A p-type silicon layer **416** is then transferred and bonded to silicon oxide layer **414**. (See step (e).) A mesa **418** is then etched into layers **410**, **414** and **416** and electrodes **420** are deposited on n-type silicon layer **402** and p-type silicon layer **416**. (See step (f).) As shown in FIGS. 1 and 3, the electrode on the p-type silicon layer may define a central opening for the light to go through. The electrode formation may be done after surface passivation using PECVD oxide or grown oxide or nitride. Via holes for metal contacts may be desirable if passivation is used. The positions of p-type and n-type silicon can be exchanged.

In some embodiments, as shown, for example, in FIGS. 1 and 4, the PIN diodes are fabricated on a solid semiconductor-on-insulator support. However, in other embodiments, the nanomembrane stack can be transferred to a flexible substrate (e.g., a plastic film), to provide flexible photodetectors and imagers and to allow light coupled from the backside of the PIN diodes. If a spherically formed flexible substrate is used, an artificial eye or similar device can be made.

The nanomembrane transfer process of steps (c) and (e) in FIG. 4 may be carried out as follows. The intrinsic layer may be fabricated from a device substrate that includes a thin layer

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of single-crystal Ge or GeSi supported on a sacrificial layer (e.g., a buried oxide layer). The intrinsic layer is then released from the sacrificial layer by removing (e.g., etching) the sacrificial layer, lifting the released layer and transferring the released layer. Lifting the released layer may be carried out by contacting the released layer with a host substrate or a tape which can be vaporized upon low-temperature heating after finishing transfer, to which the upper surface of the released layer adheres. In some embodiments, the host substrate itself forms part of the PIN diode. For example, the host substrate may be an n- or p-doped silicon layer with a native oxide on its surface. In other embodiments, the host substrate provides a temporary support on which the released layer is transported before being transferred to an n- or p-doped silicon layer with a native oxide on its surface. A similar process may be used to form and transfer a released n- or p-type silicon layer. The host substrate is generally characterized by at least one surface to which the released layer adheres. Generally, the host substrate will be coated with an adhesive coating to promote adhesion of the released layer.

For the purposes of this disclosure and unless otherwise specified, “a” or “an” means “one or more”. All patents, applications, references and publications cited herein are incorporated by reference in their entirety to the same extent as if they were individually incorporated by reference.

While the principles of this invention have been described in connection with specific embodiments, it should be understood clearly that these descriptions are made only by way of example and are not intended to limit the scope of the invention.

What is claimed is:

1. A PIN diode comprising:
 - (a) a layer of n-type silicon;
 - (b) a first tunneling barrier layer of silicon dioxide disposed over the layer of n-type silicon;
 - (c) no more than a single layer of single-crystal intrinsic semiconducting material disposed over the first tunneling barrier layer;
 - (d) a second tunneling barrier layer of silicon dioxide disposed over the layer of single-crystal intrinsic semiconducting material; and
 - (e) a layer of p-type silicon disposed over the second tunneling barrier layer,
 wherein the first and second tunneling barrier layers are each continuous silicon dioxide layers.
2. The PIN diode of claim 1, further comprising a first electrode electrically coupled to the layer of n-type silicon and a second electrode electrically coupled to the layer of p-type silicon.
3. The PIN diode of claim 2, wherein a voltage source is connected to the first and second electrodes to provide a photodetector.
4. The PIN diode of claim 1, wherein the layer of single-crystal intrinsic semiconducting material has a thickness of no more than about 2000 nm.
5. The PIN diode of claim 1, wherein the layer of single-crystal intrinsic semiconducting material has a thickness of no more than about 200 nm.
6. The PIN diode of claim 1, wherein the layer of single-crystal intrinsic semiconducting material is a single-crystal layer of intrinsic germanium.
7. The PIN diode of claim 6, wherein the layer of single-crystal intrinsic germanium has a thickness of no more than about 1000 nm.
8. The PIN diode of claim 6, wherein the layer of single-crystal intrinsic germanium has a thickness of no more than about 500 nm.

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9. The PIN diode of claim 6, wherein the layer of n-type silicon and the layer of p-type silicon are single-crystal layers with thicknesses of no more than about 1000 nm.

10. The PIN diode of claim 6, wherein the layer of n-type silicon and the layer of p-type silicon are single-crystal layers with thicknesses of no more than about 500 nm.

11. The PIN diode of claim 7, wherein the first and second tunneling barrier layers have a thickness of no more than about 10 nm.

12. The PIN diode of claim 1, wherein the layer of single-crystal intrinsic semiconducting material is a layer of single-crystal intrinsic germanium-silicon alloy.

13. The PIN diode of claim 12, wherein the layer of single-crystal intrinsic germanium-silicon alloy has a thickness of no more than about 2000 nm.

14. The PIN diode of claim 12, wherein the layer of n-type silicon and the layer of p-type silicon are single-crystal layers with thicknesses of no more than about 1000 nm.

15. The PIN diode of claim 14, wherein the first and second tunneling barrier layers have a thickness of no more than about 10 nm.

16. A photodetector array comprising a plurality of PIN diodes according to claim 3, arranged in an array.

17. The photodetector array of claim 16, further comprising at least one optical filter disposed over one or more of the plurality of PIN diodes.

18. An image sensor comprising the photodetector array of claim 16 and further comprising a CMOS circuit coupled to the photodetector array.

19. A PIN diode comprising:
 - (a) a layer of n-type silicon having a thickness of no more than about 1000 nm;
 - (b) a first tunneling barrier layer of silicon dioxide disposed over the layer of n-type silicon;
 - (c) no more than a single layer of single-crystal intrinsic germanium having a thickness of no more than about 2000 nm disposed over the first tunneling barrier layer;
 - (d) a second tunneling barrier layer of silicon dioxide disposed over the layer of single-crystal intrinsic germanium; and
 - (e) a layer of p-type silicon having a thickness of no more than about 1000 nm disposed over the second tunneling barrier layer,
 wherein the first and second tunneling barrier layers are each continuous silicon dioxide layers.

20. The PIN diode of claim 19, wherein the layers of n-type and p-type silicon have thicknesses of no more than about 500 nm and the layer of single-crystal intrinsic germanium has a thickness of no more than about 200 nm.

21. The PIN diode of claim 19, wherein a first electrode is electrically coupled to the layer of n-type silicon and a second electrode is electrically coupled to the layer of p-type silicon and a voltage source is connected to the first and second electrodes to provide a photodetector.

22. A photodetector array comprising a plurality of PIN diodes according to claim 21, arranged in an array.

23. The photodetector array of claim 22, further comprising at least one optical filter disposed over one or more of the plurality of PIN diodes.

24. An image sensor comprising the photodetector array of claim 22 and further comprising a CMOS circuit coupled to the photodetector array.

25. A PIN diode comprising:
 - (a) a layer of n-type silicon having a thickness of no more than about 1000 nm;
 - (b) a first tunneling barrier layer of silicon dioxide disposed over the layer of n-type silicon;

- (c) no more than a single layer of single-crystal intrinsic germanium-silicon alloy having a thickness of no more than about 2000 nm disposed over the first-tunneling barrier layer;
- (d) a second tunneling barrier layer of silicon dioxide disposed over the layer of single-crystal intrinsic germanium-silicon alloy; and
- (e) a layer of p-type silicon having a thickness of no more than about 1000 nm disposed over the second tunneling barrier layer,
- wherein the first and second tunneling barrier layers are each continuous silicon dioxide layers.

26. The PIN diode of claim 25, wherein the layers of n-type and p-type silicon have thicknesses of no more than about 500 nm and the layer of single-crystal intrinsic germanium-silicon alloy has a thickness of no more than about 200 nm.

27. The PIN diode of claim 25, wherein a first electrode is electrically coupled to the layer of n-type silicon and a second electrode is electrically coupled to the layer of p-type silicon and a voltage source is connected to the first and second electrodes to provide a photodetector.

28. A photodetector array comprising a plurality of PIN diodes according to claim 27, arranged in an array.

29. The photodetector array of claim 28, further comprising at least one optical filter disposed over one or more of the plurality of PIN diodes.

30. An image sensor comprising the photodetector array of claim 28 and further comprising a CMOS circuit coupled to the photodetector array.

31. A PIN diode comprising:

- (a) a layer of n-type silicon;
- (b) a first tunneling barrier layer of silicon dioxide disposed over the layer of n-type silicon;
- (c) a layer of single-crystal intrinsic semiconducting material disposed over the first tunneling barrier layer;
- (d) a second tunneling barrier layer of silicon dioxide disposed over the layer of single-crystal intrinsic semiconducting material; and
- (e) a layer of p-type silicon disposed over the second tunneling barrier layer, wherein the layer of single-crystal intrinsic semiconducting material substantially spans the length of the layer of p-type silicon, further wherein the layer of single-crystal intrinsic semiconducting material is in direct contact with the first tunneling barrier layer, the second tunneling barrier layer, or both, and further wherein the first and second tunneling barrier layers are each continuous silicon dioxide layers.

32. The PIN diode of claim 31, wherein the layer of n-type silicon and the layer of p-type silicon each have a thickness of

no more than about 1000 nm, and further wherein the single layer of single-crystal intrinsic semiconducting material is a single layer of single-crystal intrinsic germanium having a thickness of no more than about 2000 nm.

33. The PIN diode of claim 31, wherein the layer of n-type silicon and the layer of p-type silicon each have a thickness of no more than about 1000 nm, and further wherein the single layer of single-crystal intrinsic semiconducting material is a single layer of single-crystal intrinsic germanium-silicon alloy having a thickness of no more than about 2000 nm.

34. A PIN diode comprising:

- (a) a layer of n-type silicon;
- (b) a first tunneling barrier layer of silicon dioxide disposed over the layer of n-type silicon;
- (c) a layer of single-crystal intrinsic semiconducting material disposed over the first tunneling barrier layer;
- (d) a second tunneling barrier layer of silicon dioxide disposed over the layer of single-crystal intrinsic semiconducting material; and
- (e) a layer of p-type silicon disposed over the second tunneling barrier layer; wherein the layer of single-crystal intrinsic semiconducting material runs along an axis running parallel to and between the first tunneling barrier layer and the second tunneling barrier layer, further wherein there is no more than a single layer of the single-crystal intrinsic semiconducting material running along the axis between the first tunneling barrier layer and the second tunneling barrier layer, and further wherein the first and second tunneling barrier layers are each continuous silicon dioxide layers.

35. The PIN diode of claim 34, wherein the layer of single-crystal intrinsic semiconducting material is in direct contact with the first tunneling barrier layer, the second tunneling barrier layer, or both.

36. The PIN diode of claim 1, wherein the layer of single-crystal intrinsic semiconducting material is in direct contact with the first tunneling barrier layer, the second tunneling barrier layer, or both.

37. The PIN diode of claim 19, wherein the layer of single-crystal intrinsic germanium is in direct contact with the first tunneling barrier layer, the second tunneling barrier layer, or both.

38. The PIN diode of claim 25, wherein the layer of single-crystal intrinsic germanium-silicon alloy is in direct contact with the first tunneling barrier layer, the second tunneling barrier layer, or both.