Efficient Statistical Timing Analysis of Circuits

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WARF: P06158US

View U.S. Patent No. 7,689,954 in PDF format.

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an accurate statistical timing analysis for integrated circuits.

OVERVIEW

For integrated circuits such as very large scale integrated (VLSI) circuits to work properly, signals traveling on them must arrive at their destination at the proper time. However, there are many sources of timing variations, including flaws in manufacturing, densely integrated elements and power dissipation.

Statistical methods for calculating the timing variations and signal arrival time use either a flawed assumption of linear signal delays or exponentially increase in complexity with circuit size, resulting in a slow and impractical analysis.

THE INVENTION

UW-Madison researchers have developed an accurate statistical timing analysis for integrated circuits that efficiently predicts signal delay. They created a quadratic timing model that partitions the circuit into approximately equal elements and assumes uniform properties for each element. The analysis provides information about the signal delay and determines whether it is small enough for the system to operate correctly.

APPLICATIONS

- Analyzing timing variations in integrated circuits

KEY BENEFITS

- Exhibits a linear—instead of exponential—increase in complexity with circuit size and variation sources
- Offers adjustable resolution: the user can choose the size of the divided elements, with accuracy balanced against computation time

- Provides faster analysis than Monte Carlo simulation
- Provides more accurate analysis than block-based or path-based statistical timing analysis
- Low computational cost

ADDITIONAL INFORMATION

Tech Fields
Information Technology - Software

CONTACT INFORMATION

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842.