Dynamic Bandwidth Scaling Improves Energy Efficiency

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WARF: P130143US02

View U.S. Patent No. 9,588,570 in PDF format.

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a method to determine based on workload the optimal number of I/O pins needed for digital signal processors.

OVERVIEW

3-D main memory is an emerging technology in which stacks of DRAM are situated underneath the processor. This configuration helps decrease main memory latency while allowing designers to increase main memory bandwidth. The technology was initially designed to allow streaming multimedia applications to run on digital signal processors (DSPs) found in mobile devices.

The technology also supports a larger number of input/output (I/O) pins found in processors. However, wider I/O (i.e., more pins) can waste energy and does not always translate to better performance. Finding a way to determine the best number of pins for a given workload would be advantageous.

THE INVENTION

UW–Madison researchers and others have developed a 'scheduler' to dynamically scale the number of I/O pins depending on workload characteristics. The scheduler increases main memory bandwidth during memory intensive phases of a program to reduce the number of main memory accesses, then decreases the bandwidth when it is no longer needed.

Key metrics are used to identify the optimal number of I/O pins, such as instructions per cycle, utilization of execution units and the number of consecutive cache misreads.

APPLICATIONS

- Optimizing DSPs with 3-D stacked DRAM

THE WARF ADVANTAGE

Since its founding in 1925 as the patenting and licensing organization for the University of Wisconsin-Madison, WARF has been working with business and industry to transform university research into products that benefit society. WARF intellectual property managers and licensing staff members are leaders in the field of university-based technology transfer. They are familiar with the intricacies of patenting, have worked with researchers in relevant disciplines, understand industries and markets, and have negotiated innovative licensing strategies to meet the individual needs of business clients.

KEY BENEFITS

- Considerably improves performance and energy efficiency

ADDITIONAL INFORMATION

Related Technologies

WARF reference number P130137US01 describes a method to improve the performance of power-constrained processors by scaling cores and resources.

WARF reference number P100298US01 describes a method for optimizing clock speed and power dissipation in multicore processors.

Tech Fields

Information Technology - Computing methods

CONTACT INFORMATION

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846.