



Efficient Statistical Timing Analysis of Circuits

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a systematic STA solution that takes into account correlations caused by global variations and path reconvergence.

Overview

For integrated circuits, including very large scale integration (VLSI) circuits, to work properly, the signals traveling along the gates and interconnects must be properly timed. Using classical case timing analysis procedures to estimate signal delays produces grossly conservative timing predictions. Statistical timing analysis (STA), which characterizes each timing delay as a random variable, offers more accurate and realistic timing predictions; however, the correlation of timing variables in a circuit must be considered to realize the full benefit of block-based STA.

The Invention

UW-Madison researchers have developed a systematic STA solution that takes into account correlations caused by global variations and path reconvergence. They extended the commonly used canonical timing model to represent all timing variables in the circuit as a weighted linear combination of a set of independent random variables. A variation vector consisting of all these weights is used to specifically represent both global and path correlation information.

Applications

- Statistical timing analysis of signal delays in integrated circuits

Key Benefits

- Treats global and path correlation simultaneously and systematically
- Provides—for the first time—a systematic and complete solution to the two correlation problems in block-based STA: path convergence and global variations
- Computationally efficient, making rapid design and testing feasible

Additional Information

For More Information About the Inventors

- [Yu Hen Hu](#)

Tech Fields

- [Information Technology : Computing methods, software & machine learning](#)

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