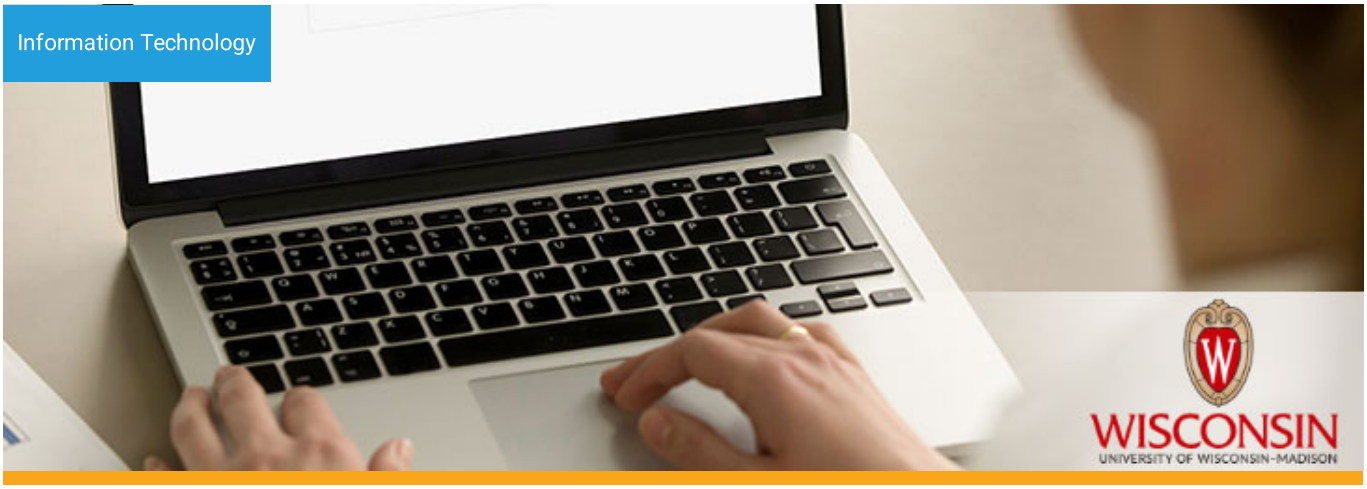
Information Technology



Low Swing Domino Logic Circuits Reduce Power Consumption in High-Performance Microprocessors

View U.S. Patent No. 7,764,087 in PDF format.

WARF: P06065US

Inventors: Volkan Kursun, Zhiyu Liu

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing techniques for reducing power consumption and enhancing immunity to noise in domino logic circuits.

Overview

Domino logic circuit techniques have been extensively applied in modern high-performance microprocessors because of their superior speed and area characteristics as compared to static complementary metal oxide semiconductor (CMOS) circuits. However, the domino logic gates frequently consume more dynamic switching power and display weaker noise immunity than static CMOS gates.

The Invention

UW-Madison researchers have developed improved low-voltage swing techniques for simultaneously reducing the active and standby mode power consumption and enhancing the immunity to noise in domino logic circuits. One circuit technique modifies the upper and lower boundaries of the voltage swing at the dynamic node while maintaining full voltage swing signals at the inputs and outputs. The circuits may utilize two power supplies and/or two ground voltages. Other circuit topologies include dynamic node low voltage swing circuits, a domino circuit with modified output voltage swing to reduce dynamic switching power consumption, multiple threshold voltage implementation of low swing domino logic circuits for suppressing the subthreshold leakage current, body-biased embodiments of low swing circuits and dynamic node low voltage swing circuits with single power supply or ground voltage.

Applications

- High-performance microprocessors

Key Benefits

- Reduces the energy required to charge and discharge the dynamic node of a domino gate without increasing the evaluation delay, unlike previous attempts to lower power consumption
- Enhances the evaluation speed
- Lowers the power consumption during the idle mode
- Maintains full voltage swing signals at the inputs and outputs for high speed operation
- Power supply and ground voltages are simultaneously optimized to minimize the power-delay product and enhance the immunity to noise

Tech Fields

- Information Technology : Hardware

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842