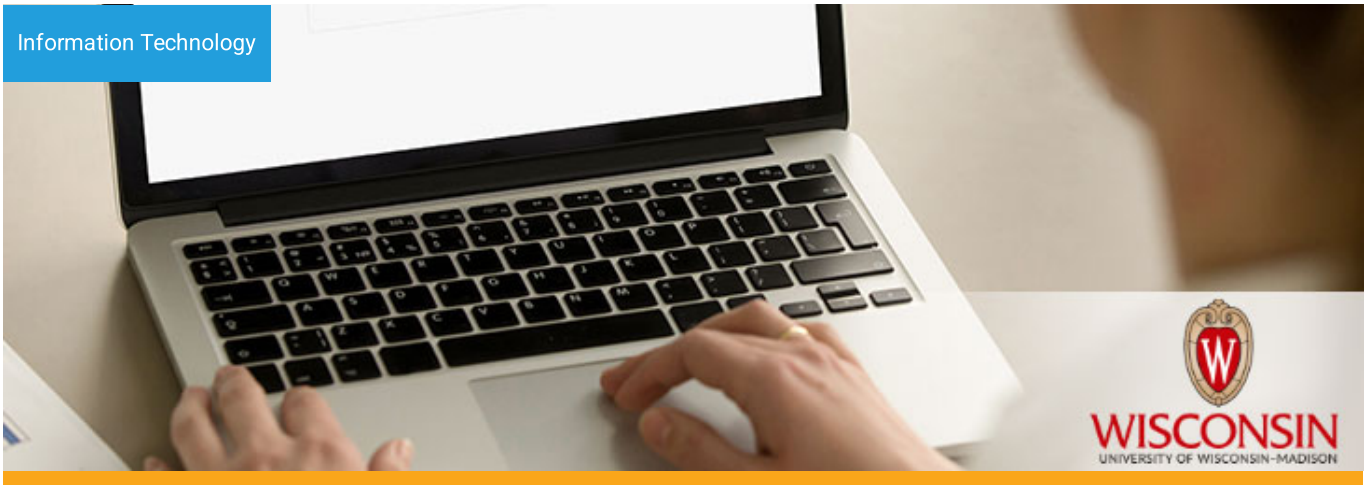
Information Technology



New Heterogeneous Cache System for Improved Efficiency in Processors

View U.S. Patent No. 8,687,453 in PDF format.

WARF: P110254US01

Inventors: Nam Sung Kim, Stark Draper

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a low voltage operating cache structure that utilizes variable size transistor cells to maximize energy efficiency in processors.

Overview

Increased circuit density in integrated circuits has intensified the need for higher efficiency with regards to both power and energy for high-performance and low-power multicore processors. Dynamic voltage and frequency scaling (DVFS) is one method used to increase processor efficiency and reduce power consumption. The voltage or frequency of a microprocessor can be adjusted using DVFS; however, if either is reduced too much, issues with system instability and reliability will occur. Large transistor cells often are used to moderate these issues, but as a result the space occupied on the chip is increased. Other methods use small transistor cells to maximize die space and improve performance, but this increases power consumption. A system that maximizes processor efficiency without sacrificing space, power consumption or performance is needed.

The Invention

UW–Madison researchers have proposed a heterogeneous cache structure that operates at reduced voltages and utilizes a combination of large and small transistors. Cache memory provides high-speed local storage for a processor that may help overcome the relatively slower access speeds available between the processor and the main solid-state memory.

The improved design provides a cache system comprising a series of addressable transistor memory cells holding digital data when powered by an operating voltage. Individual cells in the cache system may be deactivated or activated as a function of operating voltage. The cache structure is one component of the integrated circuit design, which also comprises a processor and a cache controller.

Applications

- High-performance devices that utilize cache structures
- Laptops
- Smartphones
- Microprocessors

Key Benefits

- Maximizes energy efficiency
- Maintains performance and reliability
- Reduces power consumption
- Significantly decreases the area required by large on-chip caches
- Provides a flexible tradeoff between performance and power conservation

Additional Information

Related Technologies

- See WARF reference number P100298US01 for a method of controlling the voltage at each core of a multicore processor to improve performance and efficiency.

Publications

- Ghasemi H.R., Draper S.C. and Kim N.S. 2011. Low-Voltage On-Chip Cache Architecture Using Heterogeneous Cell Sizes for High-Performance Processors. IEEE/ACM Int. Symp. on High-Performance Computer Architecture. 38-49.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846