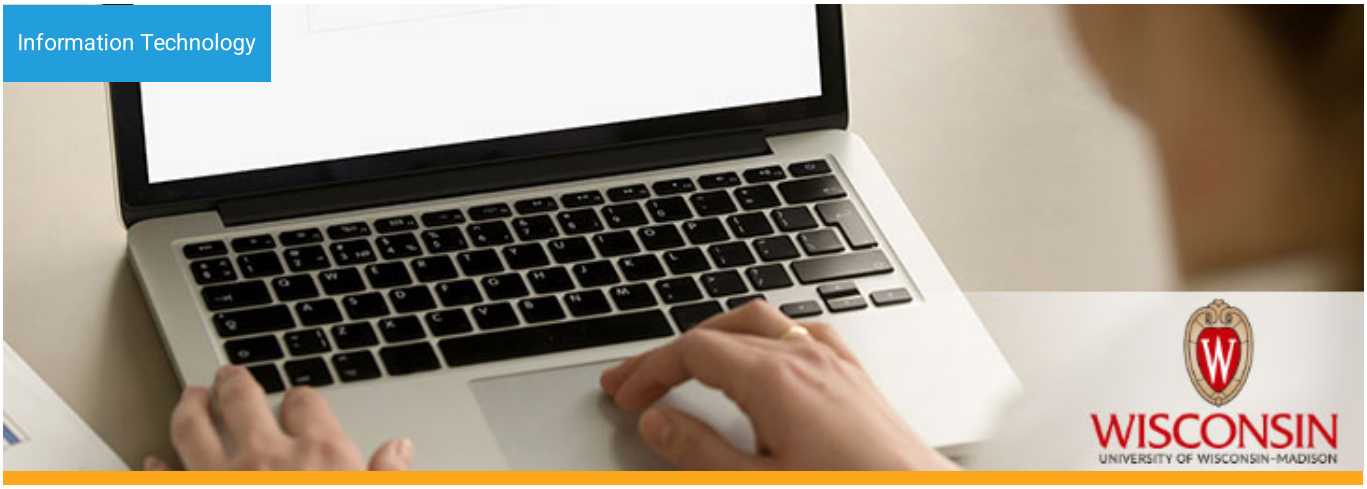
Information Technology



More Efficient Processing with Self-Invalidating IOMMU Mapping

View U.S. Patent No. 9,547,603 in PDF format.

WARF: P140029US01

Inventors: Michael Swift, Mark Hill, Arkaprava Basu

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an input-output memory management unit that reduces processor burden and memory corruption risk.

Overview

In a computer, an input-output memory management unit (IOMMU) may be positioned between the physical memory and I/O devices such as disk drives. The IOMMU provides the I/O devices with virtual addresses that are mapped to physical addresses of the physical memory. This mapping is stored in a data structure called a page table.

Furthermore, the IOMMU may include permissions limiting the reading and writing within the physical address range allocated to the I/O device, thus preventing it from accessing or corrupting the memory states of others (e.g., other I/O devices, the OS or applications).

Unfortunately, the benefits of the IOMMU in virtualization and memory corruption come at the cost of time and processor resources.

The Invention

UW–Madison researchers have developed a more efficient IOMMU. They recognized that the time required to delete a page table entry (PTE) from the page table and send the IOMMU cache deletion signal can be eliminated for most transactions.

This is done by attaching a 'removal rule' to the PTE that allows for self-deletion. The removal rule may, for example, delete the PTE after a predetermined number of memory accesses or a specified time. This significantly cuts processor time and resources required for IOMMU transactions. Also, the susceptibility of the computer to I/O device or driver errors is reduced.

Applications

- IOMMU hardware and OS/driver software

Key Benefits

- More efficient processing
- Lower risk of memory corruption
- Enables IOMMU to invalidate its own page table entries upon completion
- Removal rules are conveniently communicated and cached.
- Eases the burden on the processor

Additional Information

For More Information About the Inventors

- Michael Swift
- Mark Hill

Related Technologies

- WARF reference number P130081US01 describes a hybrid system to manage virtual memory and reduce access latency.

Tech Fields

- Information Technology : Computing methods, software & machine learning
- Information Technology : Hardware

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842