



Memory Processing Unit Boosts Performance, Cuts Energy Usage

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a system to improve memory access using 3-D stacked DRAM.

Overview

A significant amount of time and power is spent waiting for processors to retrieve instructions and data from distant levels of memory. One approach to mitigate access latency (delay) is to use a three-dimensional memory with a helper processor. In this approach, layers of memory are stacked and connected by through-silicon vias (TSVs), while the helper processor performs certain memory-intensive operations.

Although this design provides some improvements to speed and bandwidth, it continues to rely on a conventional way of organizing instructions and data. A new architecture that improves system performance and energy efficiency is still needed.

The Invention

UW–Madison researchers have developed a system to dramatically improve the benefits of 3-D die-stacking memory. Their system allows a host processor to efficiently offload entire pieces of computation for faster processing with reduced power consumption.

More specifically, memory processing unit cores are tightly coupled with sections of stacked memory layers, combined as memory ‘vaults’ in hardware. Application code is segmented into discrete partitions (‘shards’) in software for storage in the vaults. As a result, an application program is effectively broken up for execution among multiple processing cores in close proximity to memory.

Applications

- For use in 3-D-stacked processors to improve memory access
- Data intensive computing, networking and SQL database processing

Key Benefits

- Significantly higher performance and lower energy consumption
- Compatible with existing stacked DRAM designs

Stage of Development

Simulations indicate the new system can provide 3.8 times higher performance and use 13 times less energy.

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promising technologies and provides expert assistance and funding to enable achievement of commercially significant milestones. WARF believes that these technologies are especially attractive opportunities for licensing.

Additional Information

For More Information About the Inventors

- [Karthikeyan Sankaralingam](#)

Related Technologies

- [WARF reference number P09094US describes a Pipelined LookUp Grid \(PLUG\) architecture that addresses the energy efficiency and performance requirements of network devices.](#)

Tech Fields

- [Information Technology : Computing methods, software & machine learning](#)
- [Information Technology : Hardware](#)

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846

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