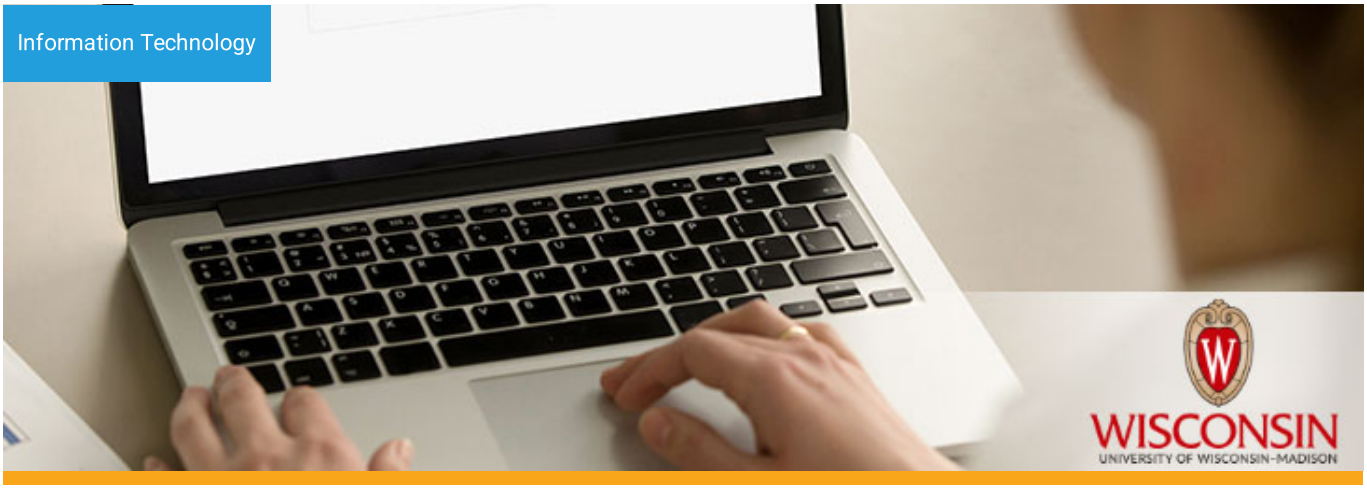
Information Technology



Spatially Programmed Logic Array Architecture

View U.S. Patent No. 10,963,302 in PDF format.

WARF: P190148US01

Inventors: Jing Li, Yue Zha

The Invention

A spatially programmed logic circuit (SPLC) array system performs spatial compilation of programs for use in the SPLCs to produce standardized compiled blocks representing predetermined portions of an SPLC. The blocks may be freely relocated in an SPLC after compilation by editing of the compiled file. Inter-block communication circuitry allows joining of blocks within an SPLC or across SPLCs to allow scalability and accommodation of different programs with efficient utilization of an SPLC for multiple programs, again without recompilation.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846