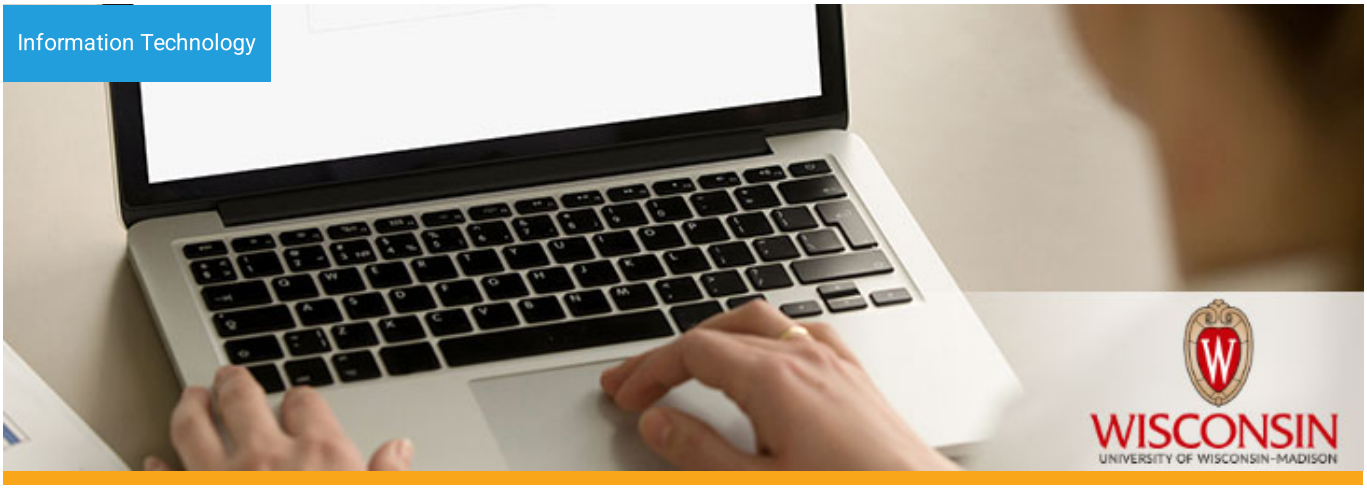
Information Technology



CACHE SYNCHRONIZATION FOR CHIPLET ACCELERATORS

View U.S. Patent No. 12,292,836 in PDF format.

WARF: P230133US01

Inventors: Matthew Sinclair, Preyesh Dalmia, Rajesh Shashi Kumar

The Invention

UW researchers have developed a novel mechanism that intelligently tracks the implicit synchronization at phase boundaries in heterogeneous systems, enabling it to be performed reactively (only when necessary) instead of proactively every time. This mechanism builds upon cache coherence protocol design for heterogeneous systems and exploits information seen by embedded microprocessors in heterogeneous systems to improve data locality and avoid extraneous data movement between phases in applications. A chiplet coherency table is used to keep track of the information in a way that can be used by the embedded microprocessor.

Additional Information

For More Information About the Inventors

- Matthew Sinclair

Tech Fields

- Information Technology : Hardware

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846