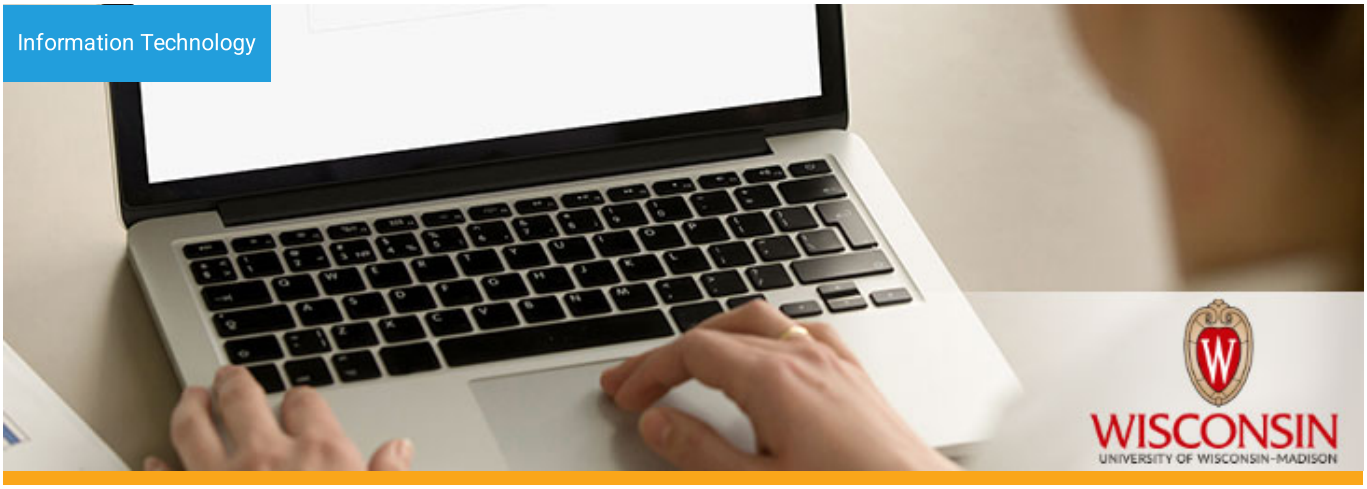
Information Technology



HETEROGENEOUS PROCESSOR WITH HIGH-SPEED DECISION TREE SCHEDULER

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Overview

The growing demand for high-performance and energy-efficient processing in machine learning, image processing, and wireless communication has led to the rise of computer architectures combining general purpose processors with specialized hardware accelerators such as digital signal processors (DSPs), image signal processors (ISPs), and fixed function accelerators performing fast Fourier transform encoding and Viterbi decoding operations. Scheduling application tasks on such heterogeneous architectures is difficult. Simple heuristics can be used but they are typically limited to specific use cases that, by their nature, fall short of an optimal solution. More sophisticated approaches, such as machine learning, incur high runtime overheads.

The Invention

UW-Madison researchers have developed a decision-tree based scheduler capable of sophisticated nanosecond scheduling decisions with relatively few calculations. The decision tree is designed to be differentiable allowing it to be pre-trained using a simulation of the heterogeneous architecture.

Tech Fields

- Information Technology : Hardware
- Information Technology : Networking & telecommunications

For current licensing status, please contact Michael Carey at mcarey@warf.org or 608-960-9867