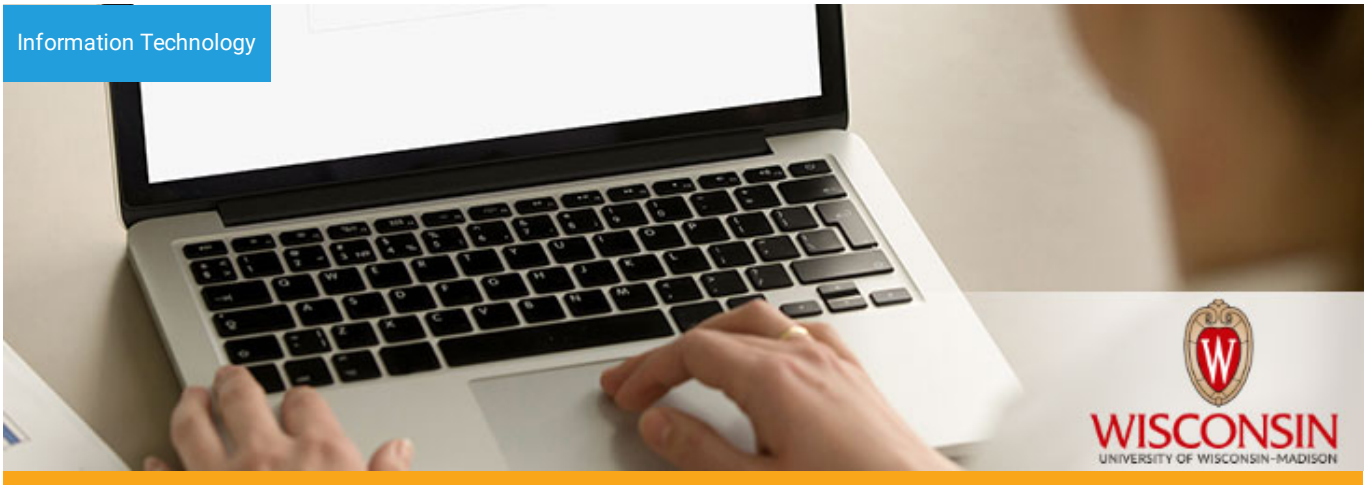
Information Technology



Decimal Floating-Point Adder

View U.S. Patent No. 7,546,328 in PDF format.

WARF: P04245US

Inventors: Michael Schulte, John Thompson, Nandini Jairam

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a decimal floating-point adder that rapidly performs decimal floating-point arithmetic, particularly addition and subtraction.

Overview

Although most people use decimal arithmetic when performing calculations, computer hardware usually only supports binary arithmetic. Numbers are typically input in decimal form, converted to binary for processing, and then converted back to decimal for output. However, converting between binary and decimal floating-point numbers is computationally intensive, and many common decimal numbers cannot be represented exactly in binary, leading to errors. Software packages for decimal arithmetic have been developed, but they are often hundreds or even thousands of times slower than binary operations in hardware.

The Invention

UW-Madison researchers have developed a decimal floating-point adder that rapidly performs decimal floating-point arithmetic, particularly addition and subtraction. The decimal floating-point adder includes an alignment unit that aligns the significands (the part of a decimal floating-point number that contains its significant digits) of two floating-point numbers so that the exponents associated with the floating-point numbers have equal values. For example, the numbers 12.3 and 4.56 could be represented as 1230×10^{-2} and 456×10^{-2}. A binary adder then adds the aligned significands. A correction unit and an output conversion unit are included in the floating-point adder to produce the final decimal floating-point number.

Applications

- Numerically intensive commercial applications

Key Benefits

- Faster than current decimal arithmetic software or hardware
- May be pipelined so that complete resultant decimal floating-point numbers are output each clock cycle

Additional Information

Related Technologies

- See WARF reference number P04398US for techniques for decimal floating-point division.
- See WARF reference number P04399US for techniques for rapid decimal multioperand addition.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842