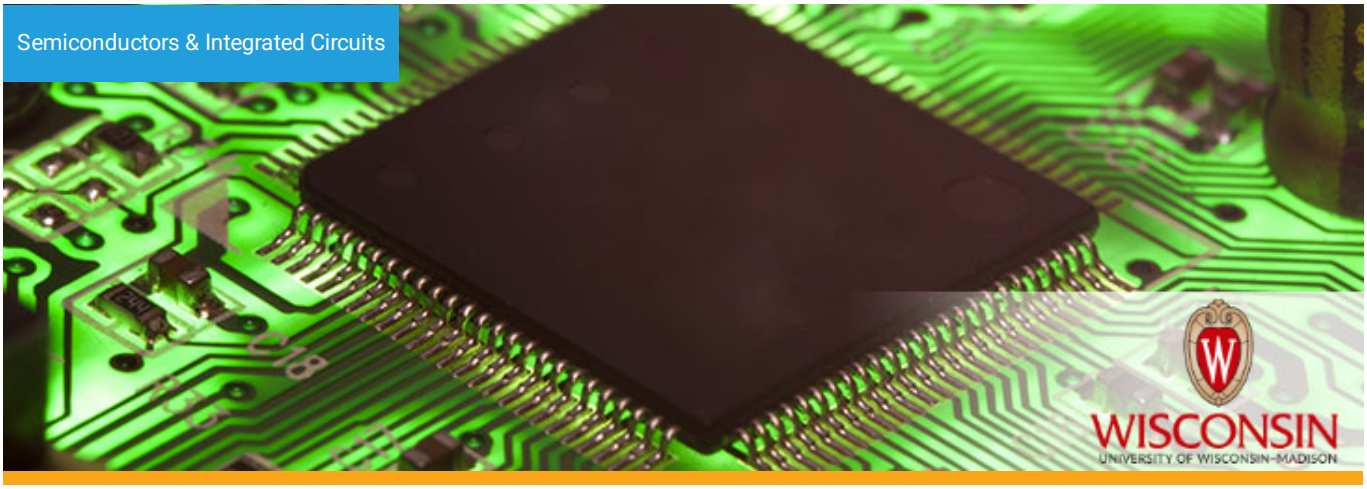

PIN Diodes for Fast Photodetection, and High-Speed, High-Resolution Imaging and Sensing

View U.S. Patent No. 7,777,290 in PDF format.

WARF: P04389US

Inventors: Max Lagally, Zhenqiang Ma

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing PIN diodes in which the intrinsic layer is Ge or SiGe and the p-type and n-type layers are silicon.

Overview

PIN diodes are semiconductor devices that include an undoped intrinsic semiconductor region between the p-type and n-type regions. These diodes are commonly integrated as photodetectors on silicon CMOS chips for imaging sensing in digital cameras.

Silicon CMOS technology offers several advantages, including ease of processing and large-scale integration; however, the speed of silicon-based PIN diodes tends to be slow. Germanium and silicon-germanium (SiGe) alloys offer promising alternative materials for high-quality, CMOS-compatible photodetectors, but the large lattice mismatch between Si and Ge has so far limited their use.

The Invention

By employing improved methods for integrating Si and Ge in thin multilayer structures, or “nanomembranes” (see WARF reference number P04286US), UW-Madison researchers have created PIN diodes in which the intrinsic layer is Ge or SiGe and the p-type and n-type layers are silicon. In some applications, these nanomembrane PIN diodes are fabricated on a solid silicon-on-insulator support. In others, the nanomembranes are released from the support and transferred to flexible substrates, such as plastic films.

Applications

- Digital imaging, such as as digital cameras and video cameras

Key Benefits

- Promises to increase the resolution and readout speed of digital imaging technologies such as digital cameras and video cameras
- Germanium absorbs light more efficiently over a wider spectrum than silicon
- Nanomembranes can be transferred to plastic films and other flexible substrates to provide flexible photodetectors and image sensors
- Fully compatible with silicon CMOS technology
- Fabrication technique achieves desired strain levels in device layers without introducing defects

Additional Information

For More Information About the Inventors

- Max Lagally
- Zhenqiang Ma

Related Technologies

- See WARF reference number P04286US for a new approach for creating a strained layer of silicon that takes advantage of the commercial availability of silicon-on-insulator (SOI) substrates.

Tech Fields

- Analytical Instrumentation, Methods & Materials : Sensors
- Semiconductors & Integrated Circuits : Design & fabrication

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846