Analytical Instrumentation, Methods & Materials

Multilayer Si/SiO_2 Semiconductors for Photoelectric Device Fabrication

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WARF: P06013US

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an improved method for the manufacturing of quantum-well photoelectric devices.

Overview

Computer chips, composed of silicon (Si) semiconductors, store and transmit information as electrons. The negative charge on electrons, however, hinders the speed with which information can be transmitted. Scientists have proposed the use of photons to store and transmit information because the discrete packets of energy have a neutral charge and propagate through any transparent medium or vacuum. Currently, an external source of photons, such as a quantum cascade laser, is needed to operate photoelectric devices.

The quantum cascade laser commonly is fabricated from direct band gap semiconductors using gallium/arsenide and aluminum/gallium/arsenide layers. These lasers have limited applications because they do not operate at room temperature and are restricted to infrared wavelengths.

UW-Madison researchers previously developed a method for increasing the mobility of electrons in Si semiconductors by straining the layers (see WARF reference number P04286US). In this process, a layer is grown on a silicon-on-insulator (SOI) substrate then etched from the substrate surface, creating an elastic strain in the layer. The growing and etching steps are repeated many times to strain and relax alternate layers of the semiconductor. The strain on the Si layer increases the mobility of electrons, enabling the semiconductor to operate faster.

The Invention

UW-Madison researchers have developed an improved method for manufacturing quantum-well photoelectric devices from monocrystalline semiconductor layers. The proposed invention aims to address the limitation of current technology with the use of Si charge carrying layers in between silicon dioxide (SiO_2) barrier layers, allowing operation at room temperature and with wavelengths in the visible region. The method used to fabricate these layers is similar to the previously developed technology except a different barrier material is used to promote electron confinement.

This method uses standard integrated-circuit deposition techniques and strain-symmetrization to produce superior virtual substrates upon which multiple layers are grown. The process starts with the SOI substrate, a well characterized and developed technology commonly used in the integrated-circuit industry to fabricate Si computer chips. The SOI base is thinned and smoothed using chemical or mechanical processes. The alternating silicon/silicon dioxide layers then are grown on the SOI using standard deposition techniques. The strain produced by the lattice constants of the two different materials is relieved by physically removing the layers from the SOI, creating a virtual substrate.

The multiple growth and removal of the multilayer structure reduces the amount of defects in the crystal lattice, resulting in increased device power. More layers can be grown on the virtual substrate to produce a component layer, but the number of grown layers is limited

to reduce imperfections in the crystal lattice. The multilayer structures then can be annealed to produce stacks of Si semiconductor of the desired thickness. These semiconductors can be used to produce inexpensive and easily integrated quantum-well photoelectric devices, which have potential applications in chemical sensors, LEDs and all digital devices.

Applications

- Sources and detectors for chip-to-chip communication; fast, flexible electronics with integrated optical communication; and integration of optical communication with fast and cheap Si-based electronics
- Sensing of gases and pollutants
- Automobile cruise control in limited visibility conditions
- Collision avoidance radar
- Industrial-process control
- Medical diagnostics

Key Benefits

- Si/SiO_2 quantum laser operates at room temperature in the visible region.
- Limiting layer growth reduces defects in the crystal lattice.
- Si layers are compatible with conventional integrated circuits.

Additional Information

For More Information About the Inventors

- Max Lagally

Related Technologies

- For more information about improved fabrication of strained silicon multilayer structures, see WARF reference number P04286US.

Publications

- Peng et al. 2007. Single-Crystal Silicon/Silicon Dioxide Multilayer Heterostructures Based on Nanomembrane Transfer. Appl. Phys. Lett. 90, 183107.

Tech Fields

- Analytical Instrumentation, Methods & Materials : Lasers
- Analytical Instrumentation, Methods & Materials : Optics
- Semiconductors & Integrated Circuits : Design & fabrication

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842