



## Progressive Random Access Scan Circuitry

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**The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a new integrated circuit test, which functions like RAS but requires less expensive hardware.**

### Overview

Very large scale integrated (VLSI) circuits are tested before use to evaluate reliability and performance. The two most common testing methods are serial-scan and random access scan (RAS). The serial-scan test is the most common, but for circuits with many transistors, it can require too much time and power consumption, often costing more to test than to create the product. RAS identifies transistors in a matrix so it can address each individually, resulting in a faster, less expensive test, but requiring expensive hardware.

### The Invention

UW-Madison researchers have developed a method and circuitry for a new integrated circuit test, called Progressive Random Access Scan (PRAS), which functions like RAS but requires less expensive hardware. PRAS combines the matrix-based data access method of RAS with the architecture of serial-scan. A static random access memory cell is hybridized with a storage element, combining functions used in RAS so that PRAS requires less space, time and energy.

### Applications

- Testing VLSI circuits

### Key Benefits

- Provides all the benefits of RAS at about the same cost as serial-scan tests
- Reduces test application time, data volume and power consumption
- Can test any type of circuit
- Allows resumption of test sequence after taking a snap-shot of circuit state
- Allows easier diagnosis of problems in circuit
- Can read circuit state without destroying it
- Operates in test mode or storage mode

### Tech Fields

- [Semiconductors & Integrated Circuits : Design & fabrication](#)

For current licensing status, please contact Jeanine Burmania at [jeanine@warf.org](mailto:jeanine@warf.org) or 608-960-9846

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