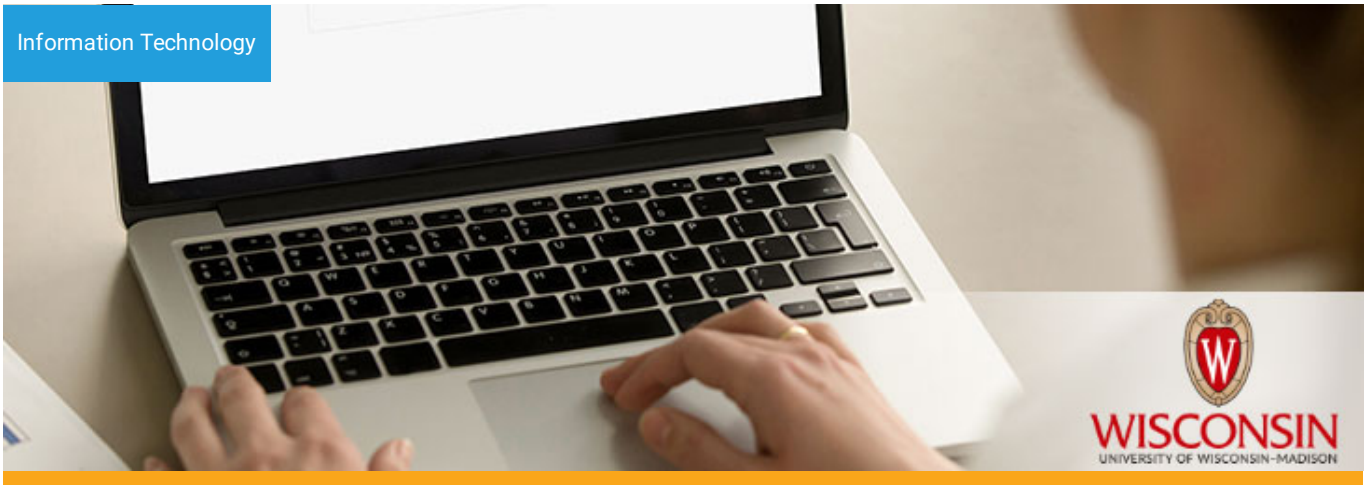
Information Technology



Signature-Based Transactional Memory for Improved Performance of Multiple Thread Microprocessors

View U.S. Patent No. 8,239,633 in PDF format.

WARF: P07519US

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing hardware that improves the performance of transactional memory (TM) programming for parallel computing in high-performance multicore microprocessors.

Overview

Multicore processor technology allows a program to utilize resources efficiently by splitting into concurrently running tasks, or threads. Problems exist when these tasks access the same data. If one thread is accessing a certain data set, another thread might only see the intermediate results of the first thread's operations. Locking the data for use by one thread at a time is a solution, but may inadvertently cause the processor to freeze or perform poorly.

Transactional memory (TM) is an emerging computer programming approach in multicore processor technology that prevents one thread from viewing incomplete results from another thread. This makes each transaction completely isolated, which leads to better performance. Hardware-based TM (HTM) provides two main capabilities over standard TM: conflict detection and version management. Conflict detection is the ability to record a read- and write-set for each transaction to identify when threads are accessing the same data. Version management is the storing of old and new values of memory to allow the system to revert to older memory in case of problems.

Most HTM systems couple conflict detection and version management together, limiting how much data can be accessed within a transaction to the size of the processor cache. Furthermore, the integration of TM with hardware data caches increases the difficulty of saving and restoring data when the operating system needs control of the processor. Decoupling conflict detection and version management capabilities is desired to enable virtualization of transactional memory for high performance processors.

The Invention

UW–Madison researchers have developed an HTM system that summarizes read- and write-sets in "signatures" for conflict detection without coupling conflict detection and version management together in memory caches. The transaction updates memory in the cache or memory, while saving the old value in a memory log for the specific thread. After each transaction, the transaction signature is cleared. These signatures can be used without requiring modifications to latency-sensitive structures such as the memory caches. Combining multiprocessor TM signatures and logs and with high performance multiple processor microprocessors improves the ability for operating systems and virtual machine monitors to virtualize transactions.

Applications

- Multiple core microprocessors and transactional memory machines

Key Benefits

- Eliminates deadlocks and poor performance from threads accessing the same data
- Decouples conflict detection and version management
- Allows any amount of transaction data copies to be saved
- Increases speed with high performance processors
- Allows operating systems and virtual machine monitors to virtualize processes easily
- Facilitates efficient saving and restoring of data

Additional Information

For More Information About the Inventors

- Mark Hill
- Michael Swift

Publications

- Yen L., Bobba J., Marty M.R., Moore K.E., Volos H., Hill M.D., Swift M.M. and Wood D.A. 2007. LogTM-SE: Decoupling Hardware Transactional Memory from Caches. In HPCA-13.

Tech Fields

- Information Technology : Hardware

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842