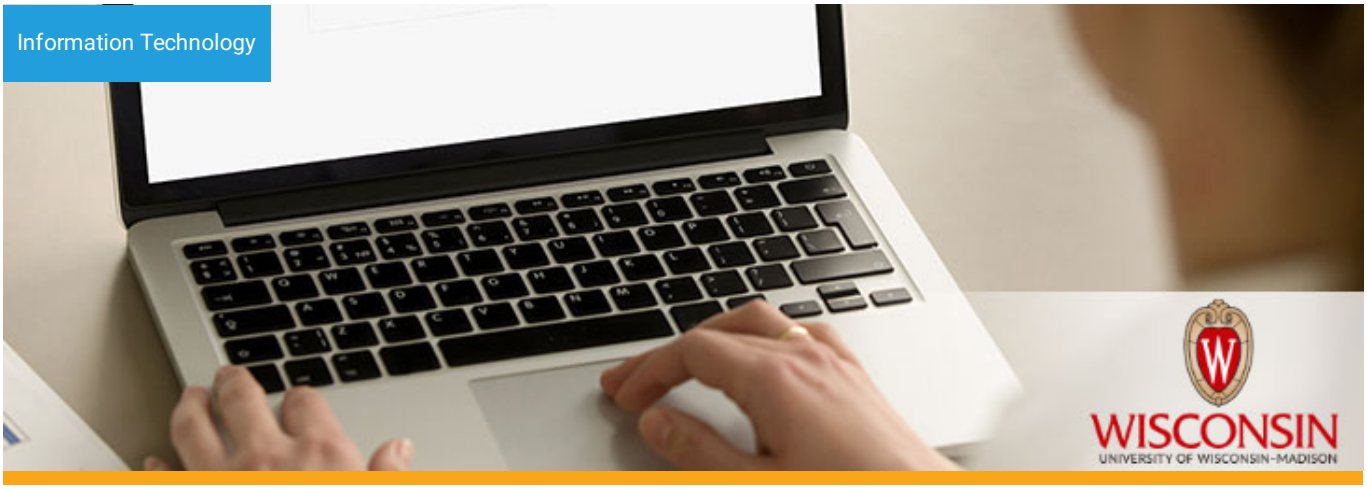
Information Technology



Optimizing Clock Speed and Power Dissipation in Multicore Processors

View U.S. Patent No. 8,281,164 in PDF format.

WARF: P100298US01

Inventors: Nam Sung Kim

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an improved method of separately controlling the voltage at each core of a multicore processor.

Overview

Multicore processors incorporate independent cores onto an integrated circuit, which allows for faster processing by distributing portions of the parallel processing task among the different cores. These processors generally utilize shared memory, which is implemented by passing messages between the different processers. As a result, the clocks of the different processes must be synchronized.

As integrated circuit technology gets smaller, the cores of multicore processors have a variety of operating properties including device delay and power leakage. This results in variations in maximum operating frequency and total power dissipation. In a typical multicore processor, the maximum operating frequency is set by the slowest core, which results in inefficient power delivery to the other cores. A trade-off between maximum operating frequency and total power dissipation may be achieved by changing the voltage applied to the cores; however, conventional multiple voltage regulators are expensive. An improved method to enhance the performance of power-constrained microprocessors is needed.

The Invention

UW-Madison researchers have developed a method to improve microprocessor performance and efficiency by tuning the power and frequency of individual cores. The transistors of the microprocessor are arranged in processing circuits, each providing local power control at each of the cores and a clock input to synchronize the clock speed of the cores. The local power controls are used to lower the maximum operating frequency of the cores to match the maximum operating frequency of the slowest core, which reduces power consumption to well below the power constraint of the system. Then, the maximum operating frequencies of all the cores can be raised with an increase in the global supply voltage until the power constraint of the system is met.

Applications

- Microprocessor architecture and design

Key Benefits

- Improves processor efficiency, operating frequency and performance
- Eliminates need for multiple, expensive voltage regulators
- Reduces electricity consumption

Technology Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846