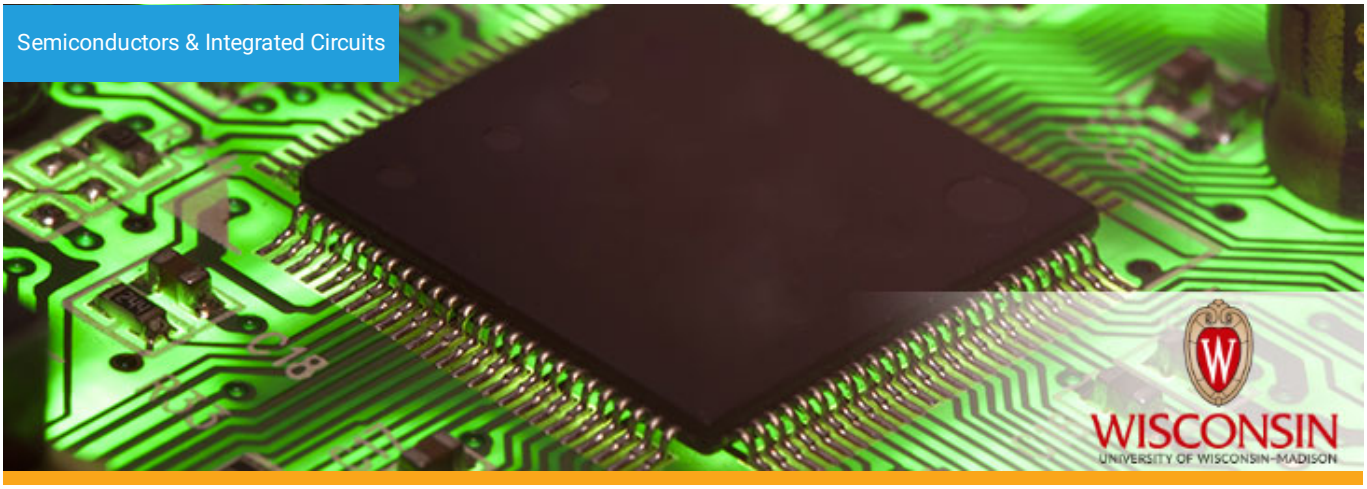
Semiconductors & Integrated Circuits



Wrapper Cell for Hierarchical System-on-Chip Testing

View U.S. Patent No. 8,533,548 in PDF format.

WARF: P110103US01

Inventors: Kewal Saluja, Kyuchull Kim

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a low-area wrapper cell design to test system-on-chip circuits with hierarchy.

Overview

Complex integrated circuits must be individually tested during manufacturing. System-on-chip (SoC) circuits combine multiple functional elements on a single substrate. For example, such systems may combine digital, analog, mixed signal and radiofrequency functional elements to produce a more complex device such as a microcontroller or cell phone. Modern SoC designs contain multiple levels of hierarchy due to functional and performance requirements.

Circuits known as “wrapper cells” are embedded within integrated circuits to allow isolated testing of individual internal functional elements. Wrapper cells allow monitoring and injection of signals at the interconnections between functional elements. Conventional wrapper cells do not permit simultaneous testing of the parent and child cores within a hierarchal circuit. A need exists for improved wrapper cells for hierarchical SoC testing.

The Invention

UW–Madison researchers have developed an improved wrapper cell design for hierarchical integrated circuits with significantly reduced complexity as compared to currently available designs. The improved design may reduce area of the integrated circuit by approximately 13 to 23 percent through reduced gate count and simplified wiring. In addition, the improved design makes it possible to use the same wrapper cell for both input and output data monitoring, which helps reduce the cost of the cell library. The design is simplified through eliminating a multiplexer and providing fewer interconnections between elements.

Applications

- Computers
- Communication equipment
- Consumer electronic devices
- Automotive applications
- Embedded systems

Key Benefits

- Enables test access mechanism optimization and test scheduling for SoCs with hierarchical cores
- Significantly reduces integrated circuit footprint
- Allows both input and output data monitoring, resulting in cost reduction

Publications

- Kim K. and Saluja K. 2009. Low-Area Wrapper Cell Design for Hierarchical SoC Testing. J. Electron. Test. 25, 347-352.

Tech Fields

- Semiconductors & Integrated Circuits : Design & fabrication

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842