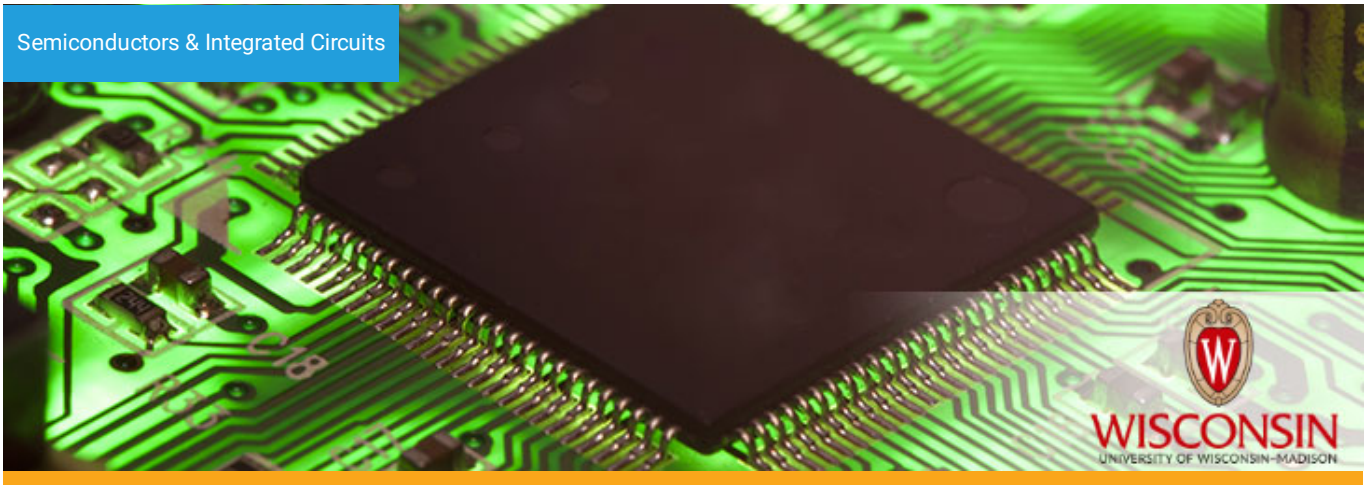
Semiconductors & Integrated Circuits



Method to Manage Active Leakage Power in Power Gated Integrated Circuits

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WARF: P110120US01

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a method to minimize active leakage power in power gated integrated circuits throughout the circuit life cycle.

Overview

Managing power consumption of integrated circuits such as microprocessors is important for conserving energy, improving battery life and reducing issues with device cooling. A common method to reduce power consumption is to place the integrated circuit in a “sleep state” or standby mode when its full capabilities are not required. The sleep state may be implemented through a set of power gating (PG) transistors placed between the input power terminal (VDD) and an effective power terminal (VVDD) of the integrated circuit. The PG device, which is activated with a sleep/wake signal, can turn the VDD supply voltage on and off an order of magnitude more quickly than an external voltage regulator, allowing more aggressive power management. The PG device often is designed to be oversized to account for worst-case power consumption and anticipated weakening of the PG transistors over time. Two mechanisms are at work, resulting in substantial power loss due to the effects of the oversized PG transistors on leakage power in the integrated circuitry being controlled.

First, the PG transistors are sized to accommodate high leakage currents when the circuit is at high operating temperatures. As the temperature of the integrated circuit drops and leakage current would be expected to decrease, the constant current operation of the PG transistors increases the voltage on the integrated circuit, reversing some of the expected drop in leakage current and decreasing potential power savings at lower temperatures. Second, the PG transistors must be sized to accommodate a decrease in current output over time. As a result, the integrated circuit operates at higher voltages than necessary during the first few years of operation, resulting in an increase in current leakage of the controlled circuitry. Power-gating techniques are needed that overcome current issues of substantial power loss due to oversized PG device sizes.

The Invention

UW–Madison researchers have developed an improved leakage power management technique using programmable power gating transistors. The method addresses the problems of oversized PG devices and active power leakage by changing the number of active power gating transistors as a function of usage-time and temperature to decrease leakage current when the PG transistors are in the on or wake state.

An integrated circuit includes multiple PG transistors connected in parallel that selectively control power to the integrated circuitry according to a sleep/wake signal used for power conservation. A transistor aging detector generates a signal reflecting aging of the power gating transistors. This signal controls the PG transistors to compensate for a decrease in PG transistor current flow as the PG transistors age. The PG transistors have different control inputs connected to the sleep/wake signal and the transistor-aging detector increases a number of control inputs connected to the sleep/wake signal as the PG transistors age. The technique decreases unnecessary leakage current early in the life of an integrated circuit by avoiding the need to oversize the PG transistors to accommodate end-of-life-cycle degradation of the transistors. As a result, supply voltage may be better tailored to minimize current leakage when the integrated circuit is young or operating at low temperatures.

Applications

- Integrated circuits that require frequent switching between sleep/wake modes

Key Benefits

- Minimizes power loss with little to no additional cost to manufacturers
- Eliminates need for conventional oversized logic gate arrays
- Reduces active leakage power by up to 10 percent

Tech Fields

- Semiconductors & Integrated Circuits : Design & fabrication
- Semiconductors & Integrated Circuits : Other semiconductor technologies

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846