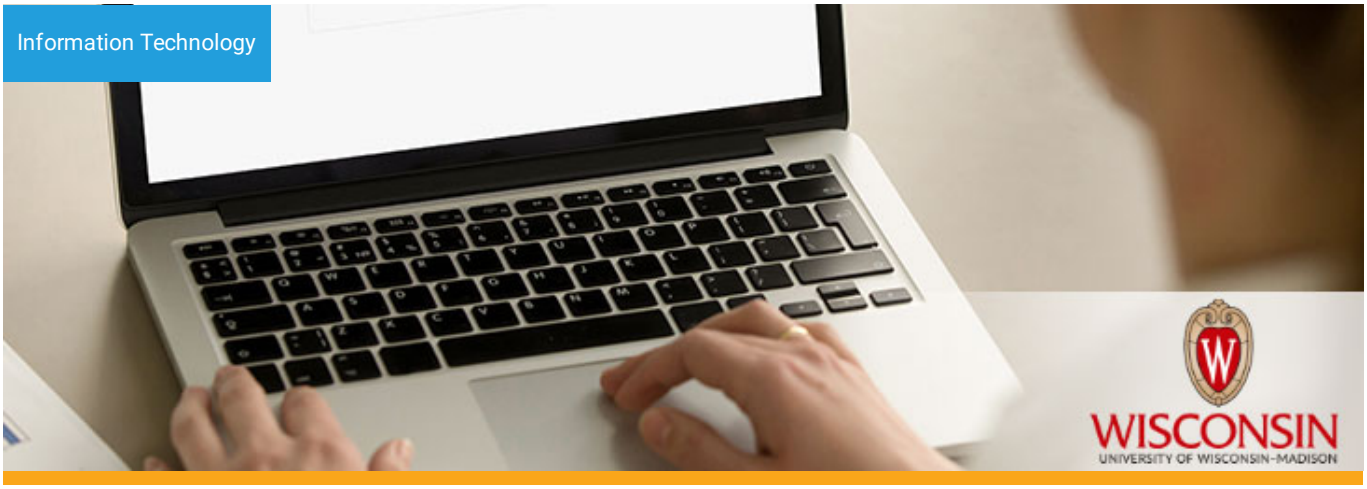
Information Technology



Precise Restarts for Handling Interrupts in Parallel Processing

View U.S. Patent No. 10,185,569 in PDF format.

WARF: P130018US01

Inventors: Gurindar Sohi, Gagan Gupta

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a method for determining the architectural state of multiprocessor systems to better respond to interrupts.

Overview

Computer 'interrupts' are signals received by a processor that cause it to switch from a present task or thread to a different one. Interrupts can be generated by hardware or software, or even execution errors (e.g., division by zero).

'Precise interruptability' refers to a processor's ability to: (i) capture the 'precise' architectural state at the time of interrupt that reflects all the instructions that preceded it and none subsequent, and (ii) resume the program as if it were not interrupted. This requires that the architectural state of the processor be well defined at the moment of interrupt so that it may be restored once the interrupt is handled.

Precise interruptability is a common feature of single processors. It has enabled a host of innovative microarchitectural techniques and is crucial to higher-level applications like debugging, fault detection and resource management, as well as performance-enhancing techniques such as speculation. However, the job is much more complex in parallel processing, where multiple processors independently execute different portions of a program at the same time. Capturing the precise architectural state of this type of system at any single instant is difficult.

The Invention

UW–Madison researchers have developed an easier method for capturing the precise architectural state of a multiprocessor system. Their approach uses computation checkpoints that hold simplified information sufficient for 'precisely restarting' after an interrupt, even though the checkpoints may not technically represent the actual state of the system at the time of interrupt.

Specifically, as the multiple processors execute different parts of a program, the method enforces a consistent order in the commitment of their results. An architectural state is determined by marking interrupts with respect to this commitment order. For example, all preceding executions in the order may be committed, while all later executions are squashed. In this way, 'precise restartability' rather than interruptability is used to reflect a total ordering of instructions that is consistent with data flow and sequence.

After an interrupt is handled, execution of the parallel portions is resumed from the architectural state.

Applications

- Implementation in multiprocessors

Key Benefits

- Precise restartability provides many of the same benefits as precise interruptability.

- Creates architectural state that is precise up to the interrupted instruction
- Handles a higher rate of interrupts
- Simplifies implementation
- Does not unduly constrain parallel execution

Additional Information

For More Information About the Inventors

- Gurindar Sohi

Related Technologies

- WARF reference number P07057US describes an automated way to parallelize the execution of a sequential computer program for multiple processors.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842