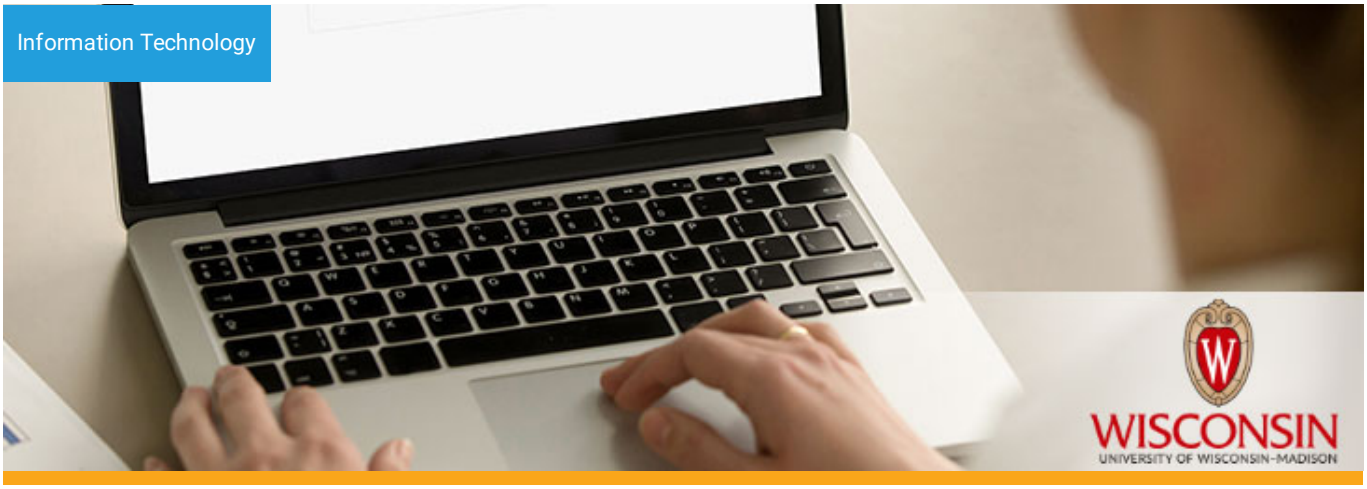
Information Technology



Managing Virtual Memory to Reduce Latency

View U.S. Patent No. 9,158,704 in PDF format.

WARF: P130081US01

Inventors: Mark Hill, Michael Swift, Arkaprava Basu

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a system that offers most of the benefits of paged virtual memory while providing extremely fast data address translation.

Overview

To execute a computer program, a processor can access memory to read or write data. The accessed data may be identified by a unique physical address. Modern systems are able to hide the physical addresses by having programs use a virtual address space that is then mapped to a physical address space. This simplifies programming, cuts down on interference and provides the illusion of more memory than is actually available.

Such virtual memory systems may employ a 'page table' that translates from virtual addresses to physical addresses. The page table translates addresses for fixed-size pages, typically four or eight KB. Recently used translations from the page table – linked pairs of virtual and physical addresses – may be cached in a hardware structure called a 'translation lookaside buffer' (TLB) to be rapidly accessible. The process of translating addresses first checks the TLB, and if the information is not found (TLB miss), traverses the page table to locate the desired translation information. Page table traversals on TLB misses can significantly delay memory accesses and increase program execution time.

The Invention

UW–Madison researchers have developed a hybrid system to manage virtual memory and reduce access latency.

The system allows some data accesses via conventional TLB/page table lookups. Other data accesses use a bypass circuit and calculate a physical address, for example, by adding an offset value to the virtual address, rather than performing a lookup. The bypass circuit is able to detect a subset of virtual addresses and translate them to physical addresses according to a stored offset between pairs.

Applications

- Upgrade for devices and systems, like search engine servers and databases, that frequently access large amounts of data in memory

Key Benefits

- Dramatically reduces address translation overhead without constraining server applications
- Extremely fast, direct address translation using a single offset value
- Allows both conventional page table translation and high-speed, offset-based translation
- Compatible with modern page table systems using TLBs or similar caches
- Amount of memory allocated to bypass is highly flexible.

- Software/dynamic control over the segregation of virtual memory between bypass and conventional TLB lookup portions

Additional Information

For More Information About the Inventors

- Mark Hill
- Michael Swift

Related Technologies

- WARF reference number P07519US describes hardware that improves the performance of transactional memory (TM) programming for parallel computing in high-performance multicore microprocessors.

Tech Fields

- Information Technology : Networking & telecommunications

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842