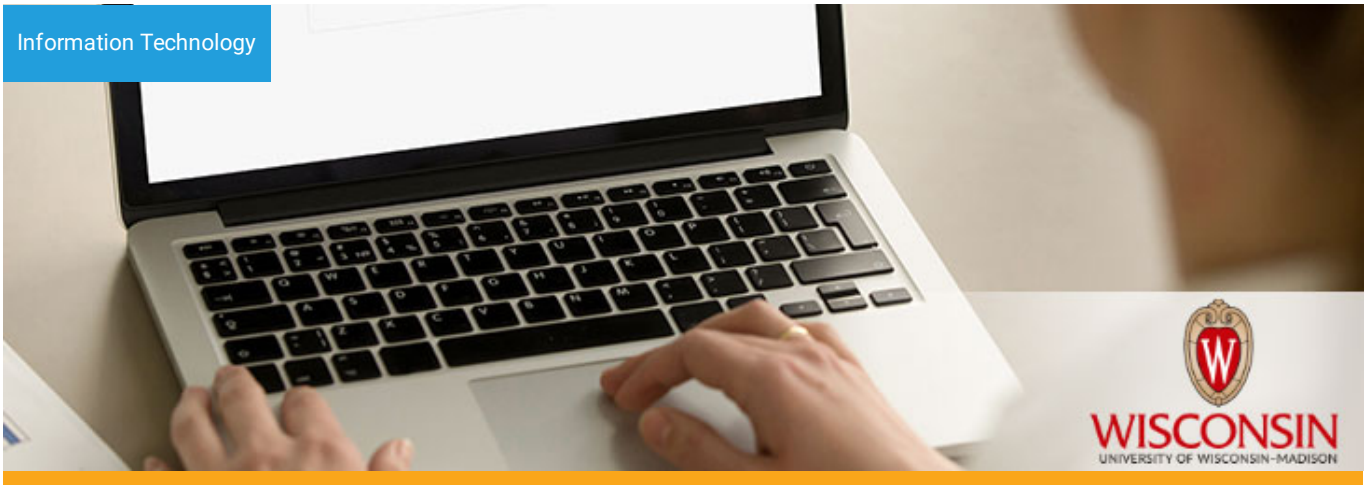
Information Technology



Predicting Logic Gate Failure

View U.S. Patent No. 9,500,705 in PDF format.

WARF: P130365US01

Inventors: Karthikeyan Sankaralingam, Raghuraman Balasubramanian

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a simple method for anticipating age-related gate failure in an integrated circuit.

Overview

Logic gates are the building blocks of integrated circuits. They use multiple transistors to receive and interpret voltage inputs, then provide outputs.

Future generations of integrated circuit microprocessors are increasingly likely to fail because of device faults at these gates. Failure resulting from age and wear can lead to degraded performance and total loss of function.

Two main strategies are used to detect faults before they occur. One technique is to monitor a small subset of gates and look for delays. However, this process can't generalize for other gates. Another technique uses a special test circuit (a 'canary') that is easy to monitor but may be inaccurate.

The Invention

UW–Madison researchers have developed a new fault prediction technique providing accuracy, generality and power efficiency. To do this, two similar circuit modules are used but one is artificially aged. Aging can be mimicked by lowering operating voltage and/or phasing a sampling clock to reduce slack time. Both approaches make the 'aged' gate more sensitive to delay. To achieve power efficiency, a novel technique is used to turn on this 'mode' at a low periodic rate.

The outputs of the two circuit modules is compared. Discrepancy in output indicates a projected failure.

Applications

- Predicting gate faults
- Higher-end processors, with applications in graphics processing units (GPUs) and high-performing servers

Key Benefits

- High accuracy
- Good detection coverage
- Low power and resource overhead
- Utilizes actual components of the target circuit
- More likely to detect infrequent errors
- Enables fault predictions further into the future
- Method is simple and can be applied to large numbers of gates without added complexity.

Additional Information

For More Information About the Inventors

- Karthikeyan Sankaralingam

Tech Fields

- Information Technology : Computing methods, software & machine learning
- Information Technology : Hardware

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846