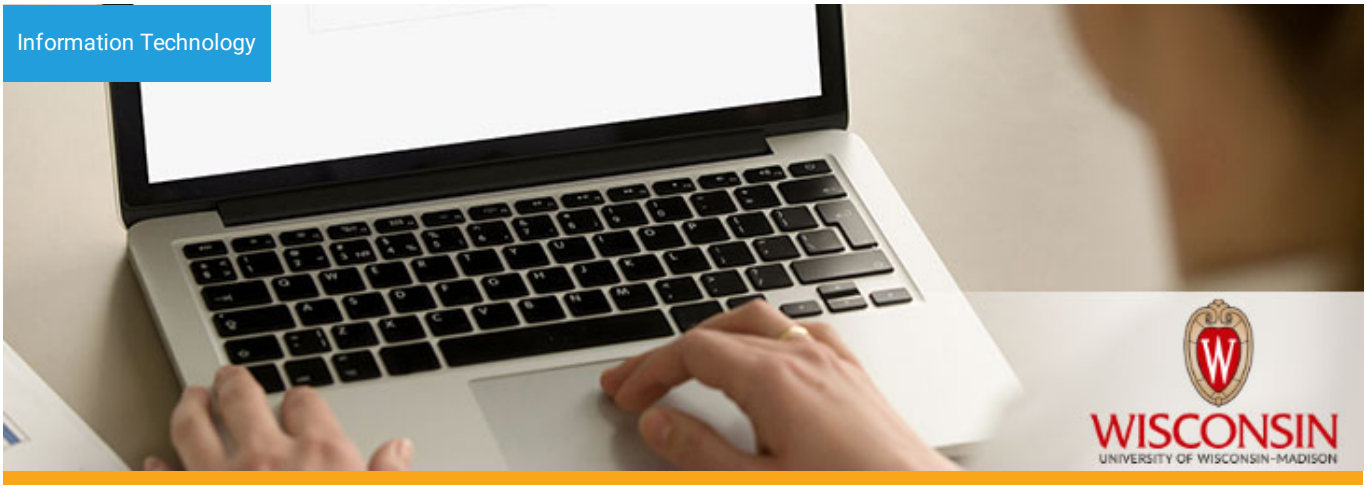
Information Technology



Memory Conserves Power, Is More Reliable

View U.S. Patent No. 9,323,614 in PDF format.

WARF: P140001US01

Inventors: Nam Sung Kim

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an improved on-chip memory structure that activates error handling as a function of operating voltage.

Overview

As circuit density increases, power efficiency has become a design priority for high-performance and low-power processors. Better energy efficiency means faster speeds and longer battery life.

One technique to boost processor efficiency is Dynamic Voltage and Frequency Scaling (DVFS), in which processor voltage and clock speed are reduced at times of low processing demand. This significantly cuts the power consumption of transistors. The lowest voltage at which memory cells can maintain their logical state is known as minimal voltage (V_{min}).

V_{min} may be reduced by increasing transistor size, but this takes up chip space. UW–Madison researchers previously addressed the problem by developing a heterogeneous cache structure that utilizes a combination of large and small transistors and operates at reduced voltages. Still, improvements are needed to balance performance and efficiency.

The Invention

A UW–Madison researcher has developed a new memory structure (e.g., for caches, SRAM, DRAM, translation lookaside buffers, etc.) that controls error handling as a function of operating voltage. In this way, errors are corrected when the memory is run at low voltage and frequency.

The new design is made of multiple independently controlled groups of memory cells, each adapted to store digital data bits and error handling bits. A memory controller monitors the circuit to determine operating voltage and look for errors in the different groups when voltage is low. The groups have different physical sizes, and therefore have differing, predetermined susceptibility to errors as a function of voltage.

Performance issues associated with error correction, such as additional access latencies, can be avoided when the memory structure is run at a higher voltage (and frequency) and errors are less likely. Also, increased latencies due to evaluating error handling bits may be hidden by reading the digital data bits speculatively and assuming no errors.

Applications

- Especially useful for battery-operated, high-performance devices
- Laptops
- Smartphones
- Microprocessors

Key Benefits

- Maximizes energy efficiency
- Maintains performance and reliability
- Reduces power consumption
- Significantly decreases the area required by large on-chip caches
- Provides a flexible tradeoff between performance and power conservation

Stage of Development

Simulations have shown promising results.

Additional Information

Related Technologies

- WARF reference number P110254US01 describes the researcher's previously developed heterogeneous cache structure.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846