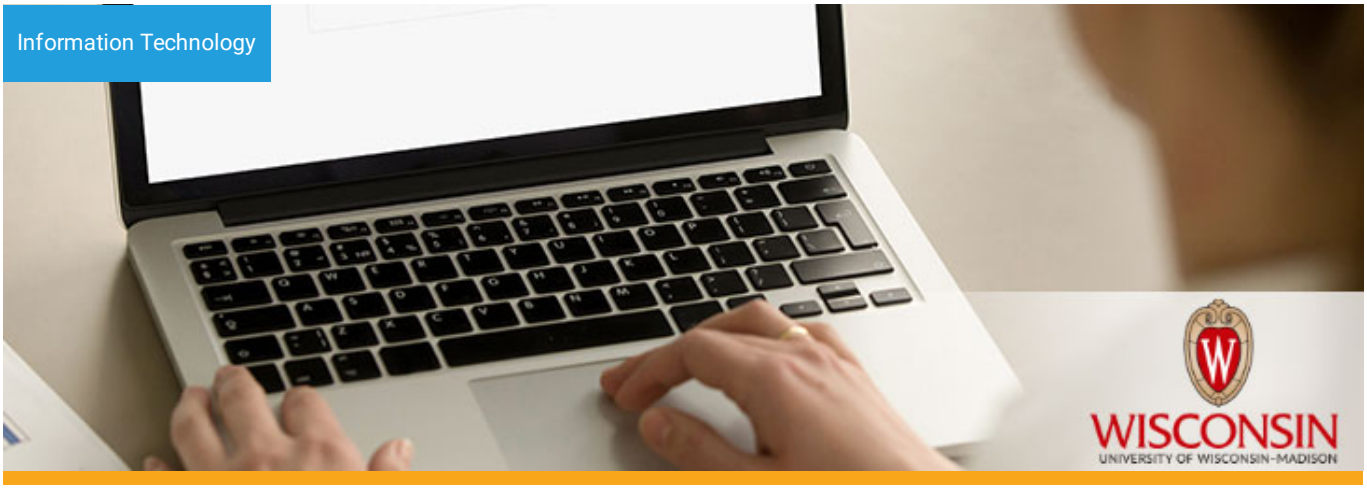
Information Technology



Energy-Efficient Parallel Processing

View U.S. Patent No. 9,519,330 in PDF format.

WARF: P140039US01

Inventors: Nam Sung Kim

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing multicore processors that save power by exploiting synchronization cycles.

Overview

In a multicore processor, the different cores share a common clock timing and operate at a synchronized frequency. Such processors are fast because their cores can work in parallel to execute different 'threads' of a program. These threads often need to modify common data. For example, airline reservation systems must read and write common data indicating the number of available seats. If the threads are not coordinated, different customers may book the same seat.

To avoid these problems, it is common to use synchronization instructions (or 'primitives') such as lock variables to coordinate threads. The lock indicates whether it is available or currently owned by a thread. When a lock is owned, a processor may 'spin,' ceasing forward progress while it waits for the lock to become available. Other synchronization primitives (like barriers and conditions) also employ this spinning technique.

While a processor is spinning, it does not perform useful work but consumes substantial power. It cannot be powered down because it must regularly check if the lock has become available. One approach is to wake the sleeping thread when the lock becomes available, but this entails multiple system calls that consume many processor cycles.

The Invention

A UW–Madison researcher has developed a technique to reduce the clock speed of spinning cores. This conserves energy during fine-grained synchronization events that would otherwise be fatally slowed by multiple system calls.

Specifically, clock dividers are provided on each core, allowing rapid changes in clock frequencies. A spinning core is slowed but still can operate in the environment of the other processors by making certain frequency adjustments. Power fluctuations that may result from abrupt clock speed changes can be minimized by disabling processor functions prior to the change.

Applications

- Multicore processors

Key Benefits

- Saves power
- Simple hardware modification
- Preserves processor core function and architectural state
- No need for multiple voltage domains for each core

- Necessary clock speed circuitry is compact, in contrast to on-chip voltage regulators.

Additional Information

Related Technologies

- WARF reference number P100298US01 describes a method to improve microprocessor performance and efficiency by tuning the power and frequency of individual cores.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846