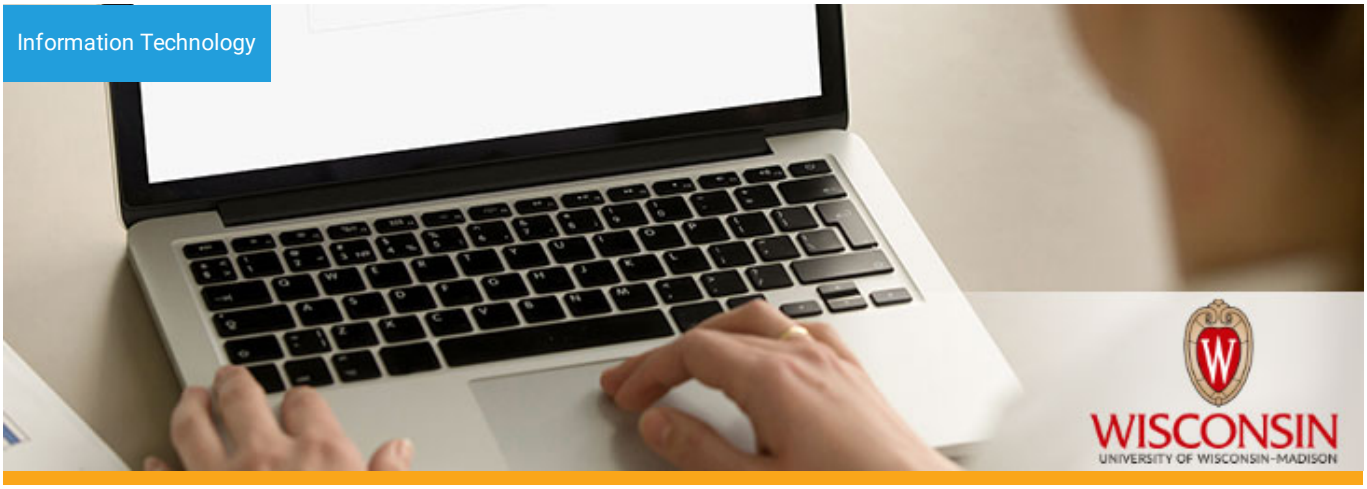
Information Technology



Computer Accelerator System Boosts Efficiency

View U.S. Patent No. 10,591,983 in PDF format.

WARF: P140164US01

Inventors: Karthikeyan Sankaralingam, Chen-Han Ho, Sung Kim

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a specialized access processor that works with a hardware accelerator for faster computer processing.

Overview

Hardware accelerators improve computer performance by allowing the main processor to off-load certain tasks, for example, processing floating-point or graphics calculations. The accelerator is designed to run some tasks faster than the main processor while omitting other capabilities.

In current practice, accelerators are tightly integrated with a main out-of-order (OOO) processor. The processor feeds data at a high rate to the accelerator, which then executes the tasks on demand. Using the main processor in this way consumes substantial power and limits the energy efficiency that otherwise would be gained from acceleration.

The Invention

UW–Madison researchers have developed a specialized memory access processor that takes over the job of feeding data to the accelerator. It is placed between the main processor and the accelerator.

The circuit is specialized for a narrow task, in this case performing memory access and address calculations. It is as fast as the main OOO processor yet more efficient. The main OOO processor – free from memory access duties – may switch to an energy conserving sleep mode until the accelerator is finished, or may move on to other tasks.

Applications

- Chips used in desktops, laptops and data center servers

Key Benefits

- Takes burden off main processor
- Improves efficiency and performance
- Helps save power
- Speed of memory access is on par with traditional OOO processor systems.
- Works with a wide variety of standard hardware accelerators
- Can be used with a versatile, high speed data flow fabric architecture

Stage of Development

Simulations have been run using industry standard benchmarks. Reductions in overall power consumption may reach 70 percent.

Additional Information

For More Information About the Inventors

- Karthikeyan Sankaralingam

Related Technologies

- WARF reference number P09094US describes a Pipelined LookUp Grid (PLUG) architecture that addresses the energy efficiency and performance requirements of network devices.

Tech Fields

- Information Technology : Computing methods, software & machine learning
- Information Technology : Hardware

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846