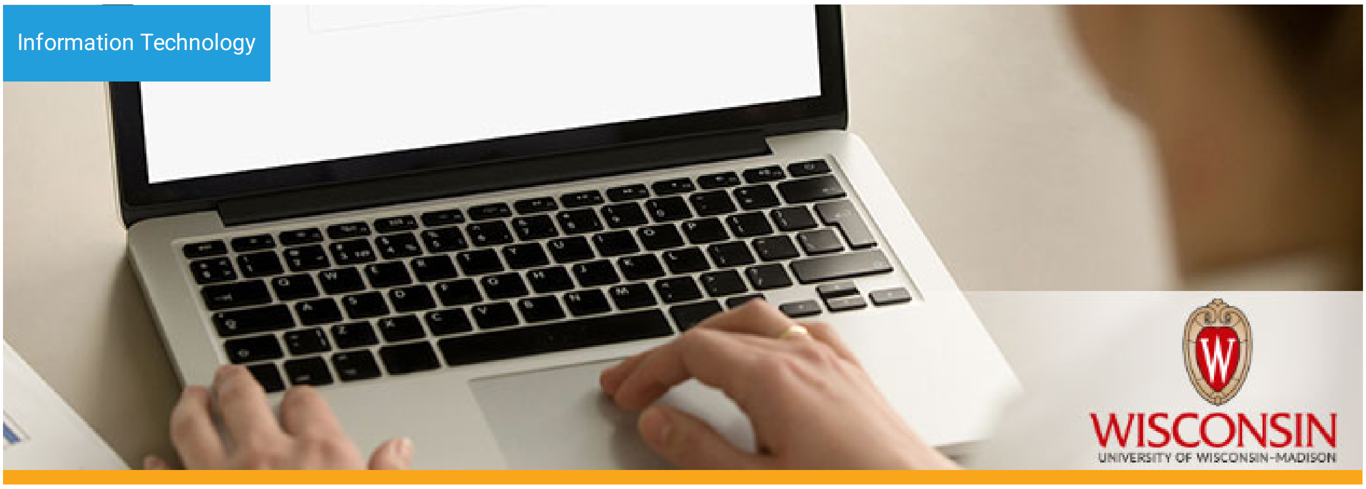

New Hardware Helps Cell Phones, Tablets Save Power

View U.S. Patent No. 9,639,328 in PDF format.

WARF: P140276US01

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing an energy-efficient multiplier circuit that provides a flexible tradeoff between power and accuracy in portable devices.

Overview

Energy efficiency is important in mobile electronics such as smart phones and tablets because of their size and reliance on battery power. At the same time, these kinds of devices must perform increasingly sophisticated tasks like speech and gesture recognition.

Such tasks require large numbers of multiplication operations. High-speed multiplications typically are handled by specialized circuits that consume lots of energy and drain battery life.

The Invention

UW–Madison researchers have developed a more energy-efficient multiplier circuit for portable electronics. The circuit performs 'dynamic truncation,' reducing the size of operands to capture their most important bits. This allows multiplication to be performed using a much smaller multiplier, significantly reducing energy consumption.

Dynamic truncation works by preserving computationally important bits and providing approximations that are satisfactory for most applications.

Applications

- Processors for wireless devices, where power is prioritized over strict accuracy

Key Benefits

- Balances power usage and accuracy
- Provides dramatic gains in energy efficiency
- Improves error reduction
- Can be implemented with standard hardware
- Simplifies multiplier circuitry

Stage of Development

The new multiplier can consume 58 percent less energy per operation, with an average computational error of about one percent. Such minor errors do not notably impact digital signal processing quality or the accuracy of classification applications.

Additional Information

Related Technologies

- WARF reference number P130132US01 describes a multiplier circuit that adjusts computing accuracy during run time to conserve energy.
- WARF reference number P120224US01 describes a method for improving GPU performance using memory-link compression.

Tech Fields

- Information Technology : Computing methods, software & machine learning
- Information Technology : Hardware

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846