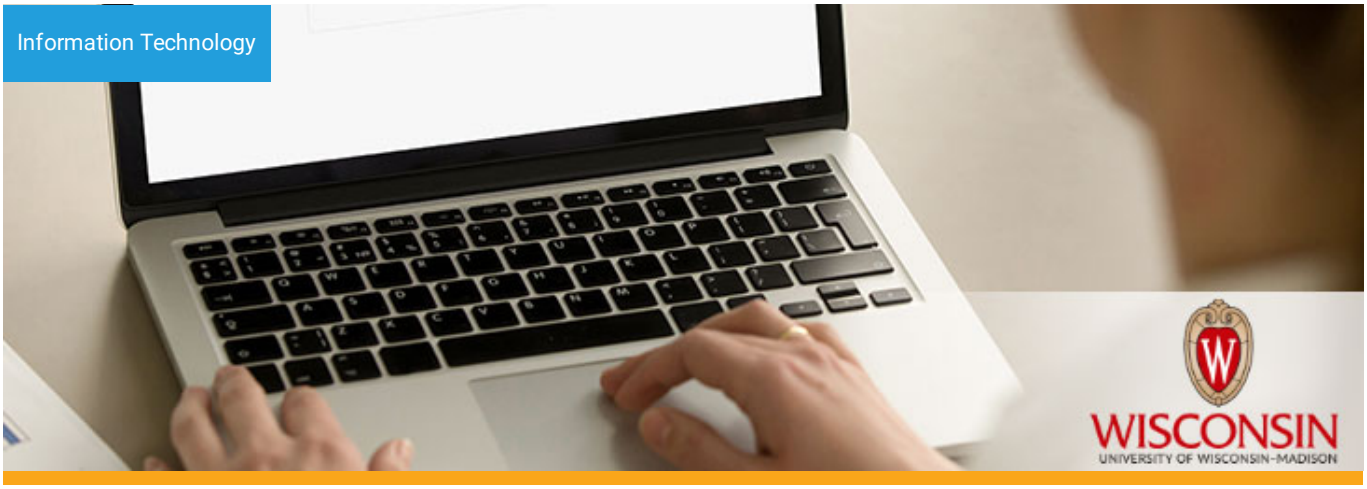
Information Technology



Intelligent Memory Fault Patching Cuts Costs

View U.S. Patent No. 9,626,297 in PDF format.

WARF: P140425US01

Inventors: Mikko Lipasti, Nam Sung Kim, David Palframan

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a method to address intermittent memory errors by leveraging preexisting memory structures.

Overview

The development of smaller, denser transistors has revolutionized computer performance but given rise to power dissipation problems, wherein a chip or part of a chip consumes more power than can effectively be cooled.

The problem generally is addressed in two ways, each with different drawbacks. When performance is not critical, the operating voltage and clock speed of the processor can be reduced, which can cause voltage-dependent memory errors. An alternative approach is to push the temperature limits of the processors, but this can lead to temperature-dependent memory errors.

A variety of techniques exist to mitigate such memory errors (e.g., incorporating more components or making larger transistors) but these techniques tend to increase the size and cost of processors and memory structures.

The Invention

UW–Madison researchers have developed a method that allows “patching” of failed memory elements using alternative memory. They determined that under normal operating conditions there is excess capacity in many redundant memory structures, thus providing a solution with little or no cost impact.

In the new method, accesses to data from faulted memory areas is diverted to a secondary memory structure. This secondary memory structure is flagged to increase the persistence of the stored data used for patching against normal updating policies.

Applications

- Intelligent memory fault patching for applications ranging from mobile devices to servers

Key Benefits

- Leverages existing hardware and mechanisms
- Implementation is noninvasive, low cost and requires little departure from modern processor designs.
- Provides significant energy savings
- Improves performance while taking up less space
- Ensures that memory structures are still functional for their original purpose

Stage of Development

Simulations have been done on industry-accepted software and benchmark programs for performance and energy comparisons.

Additional Information

Related Technologies

- WARF reference number P100298US01 describes a method for optimizing clock speed and power dissipation in multicore processors.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846