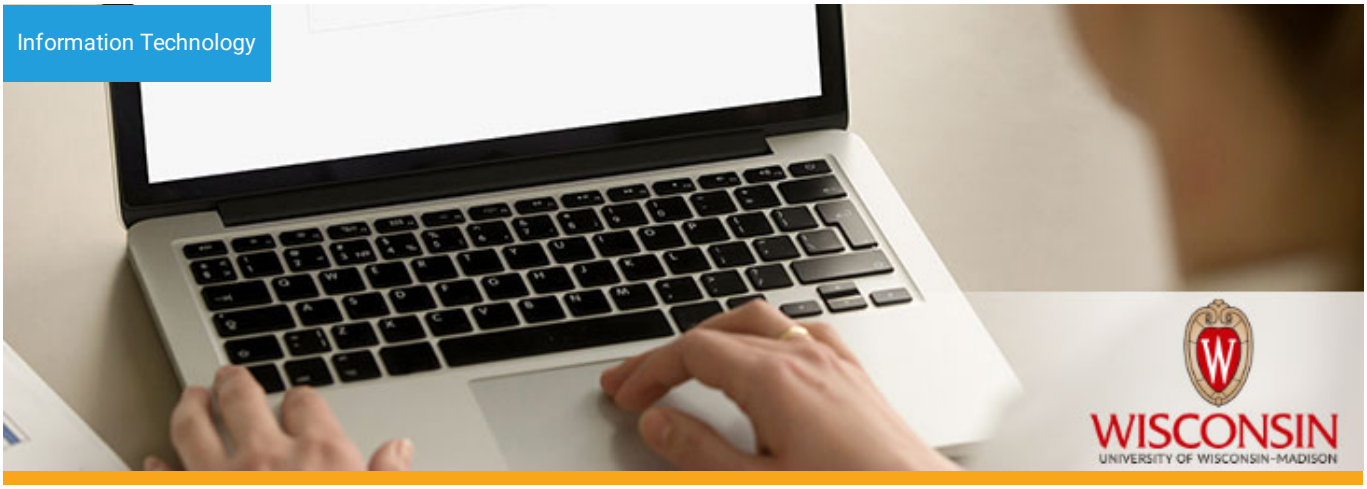
Information Technology



Predicting Computer Memory Failure

View U.S. Patent No. 9,384,858 in PDF format.

WARF: P150070US01

Inventors: Karthikeyan Sankaralingam, Amir Yazdanbakhsh, Raghuraman Balasubramanian, Anthony Nowatzki

The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a method to anticipate age-related wearout of SRAM and cache memory.

Overview

It is widely accepted that future processor technology will suffer from some degree of failure due to core aging. This failure leads to device faults. Anticipating faults before they occur can help the processor be used more strategically or alert an operator to the problem.

With increasing pressure on manufacturers to offer greater reliability and performance, new ways are being explored to identify and manage faults. UW–Madison researchers previously developed an accurate method to predict logic gate faults and run programs in a smarter way to move forward (see WARF reference number P130365US01).

An equally effective method is needed to predict faults in memory.

The Invention

The researchers have now developed a method for predicting faults in static random access memory (SRAM) and cache cells. In the new method a memory circuit is artificially aged by reducing voltage, then checked using a predetermined test vector. The vector is altered if there is memory cell failure (i.e., a value of 1 will read out as 0).

The portion of memory being checked may be small and rotated through the entire memory structure to minimize overhead.

Applications

- Software to predict memory faults
- Could be used for higher-end processors

Key Benefits

- Helps prolong the operating life of memory
- Decommissions faulty memory circuitry before more serious problems occur
- Does not disrupt processor operations
- The test is flexible and may be tailored to a particular memory architecture.
- Short prediction windows (less than a month or day) maximize processor life.
- The amount of artificial ‘aging’ can be controlled.
- Works in conjunction with methods for predicting logic gate faults
- Low overhead
- Does not change how memory is manufactured

Stage of Development

Simulations and benchmarking have been performed using standard software.

Additional Information

For More Information About the Inventors

- Karthikeyan Sankaralingam

Related Technologies

- See WARF reference number P130365US01 for more information about the researcher's method for predicting logic gate failure.

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846