



Hardware Blends Compute/Storage Capabilities, Increases Efficiency

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WARF: P150232US01

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing innovative computer architecture that uses nonvolatile memory and allows memory and processing to be closely integrated on a program-by-program basis.

Overview

Perhaps surprising to many consumers, the industry that produces compute hardware (microprocessors, graphic units, etc.) is highly disconnected from the industry that produces memory storage hardware (DRAM-based memory, Flash storage, etc.) The chips are very different in form and design, and a lot of energy and time is spent transporting data between them.

There is a need for new unified hardware that can blur the traditional boundary between computation and storage. Moreover, any potential solution must work with emerging nonvolatile memory technologies currently being developed, such as phase change memory, spin-torque transfer RAM and resistive RAM.

The Invention

A UW-Madison researcher has developed a versatile new computer architecture using interconnected tiles that can alternate between memory and computation functions. More specifically, each tile can be configured as a (i) multibit nonvolatile memory, (ii) logic gate array or (iii) routing switch. The ability to dynamically change the function of any of the tiles allows precise tailoring to workload and reduces data transfer costs.

Applications

- New architecture for use with nonvolatile memory implemented in hardware

Key Benefits

- Dramatic energy savings
- Highly versatile and dynamic

Stage of Development

A preliminary comparison indicates a 100-fold speed up and ultralow power usage due to the lack of data movement.

Publications

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Tech Fields

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