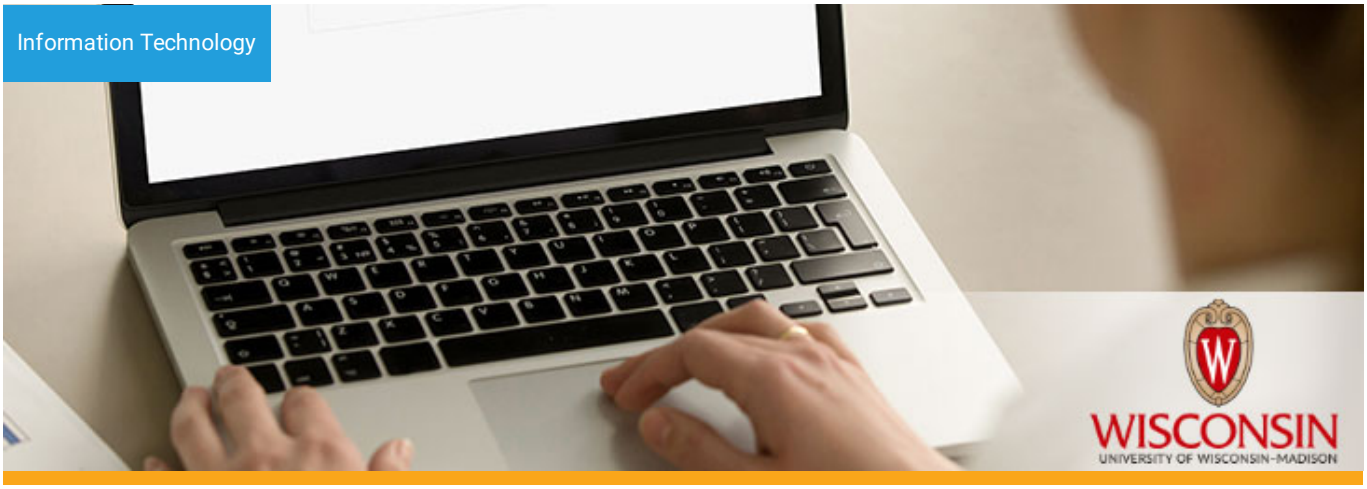
Information Technology



Encrypted Digital Circuit Description Allowing Signal Delay Simulation

View U.S. Patent No. 9,960,910 in PDF format.

WARF: P160174US01

Inventors: Parameswaran Ramanathan, Kewal Saluja

The Invention

A system for creating protected functional descriptions of integrated circuits provides encrypted gate delay information preventing deduction of gate function from gate delay but allowing simulation of the integrated circuit with accurate propagation delay calculation. Individual gate delay values may be modified so that they obscure actual gate delays but so that the modified individual gate delays total to equal the actual cumulative gate delay along a given data propagation path.

Additional Information

For More Information About the Inventors

- Parameswaran Ramanathan

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842