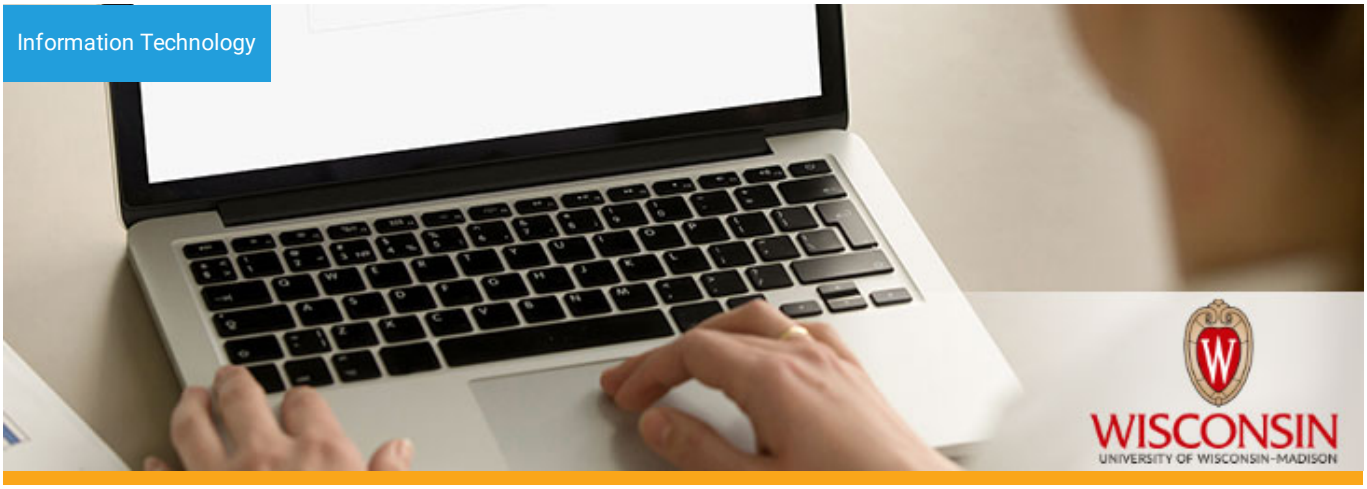
Information Technology



COMPUTER ARCHITECTURE WITH REGISTER NAME ADDRESSING AND DYNAMIC LOAD SIZE ADJUSTMENT

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The Invention

A computer architecture allows load instructions to fetch from cache memory "fat" loads having more data than necessary to satisfy execution of the load instruction, for example, loading a full cache line instead of a required word. The fat load allows load instructions having spatiotemporal locality to share the data of the fat load avoiding cache accesses. Rapid access to local data structures is provided by using base register names to directly access those structures as a proxy for the actual load base register address.

Additional Information

For More Information About the Inventors

- Gurindar Sohi

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842