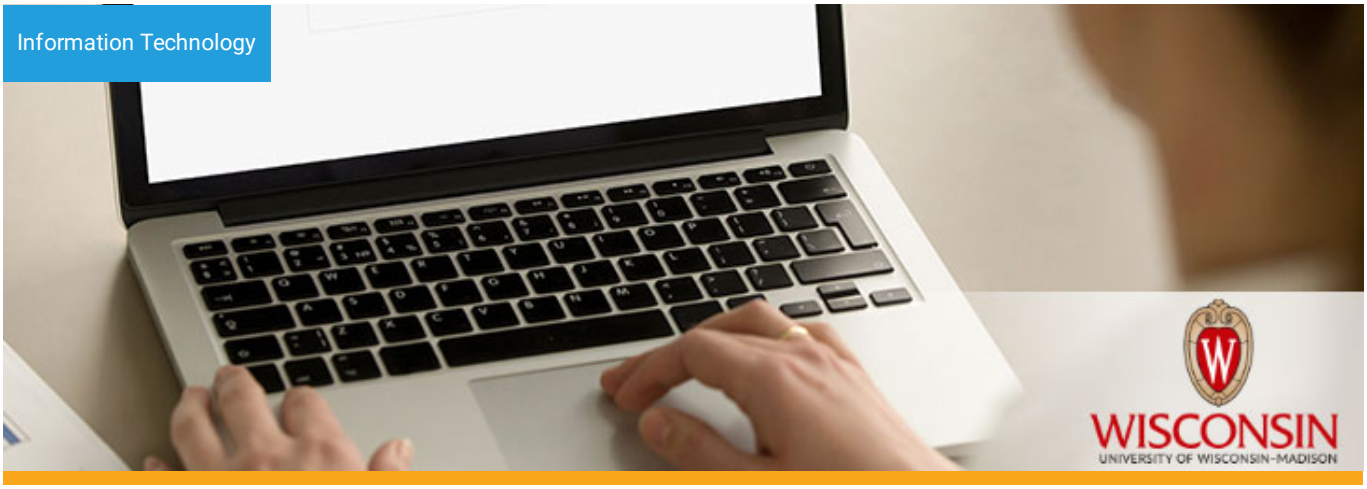
Information Technology



COMPUTER ARCHITECTURE USING PROGRAM COUNTER INDEXED DATA ADDRESS TRANSLATION

WARF: P240199US01

Inventors: Gurindar Sohi, Shyam Murthy

The Invention

UW-Madison researchers have designed a non-traditional approach to memory address translation. PC-Indexed Data Address Translation (PCAX), assists with conventional data address translation which employs a conventional Data Translation Lookaside Buffer. The approach relies on using the identity of an instruction (the instruction PC), and not on the actual data address, to obtain a page table entry for the data address that is expected to be accessed by the instruction. PCAX is intended to be used for a small subset of load instructions: those whose data translation access is expected to miss in a CDLTB. The inventors have determined that: (1) a relatively small number of instructions statically identified by their program counter (PC) values are responsible for a disproportionate number of misses in a TLB, and (2) dynamic instances of these instructions frequently access the same page table entry. Accordingly, a relatively small table indexed with the PC value of an instruction, and holding page table entry information (pairs of virtual and physical memory addresses) can be used to provide an address translation for the data that the instruction is accessing, producing an acceleration in translation time and also providing energy savings.

Additional Information

For More Information About the Inventors

- Gurindar Sohi

Tech Fields

- Information Technology : Computing methods, software & machine learning

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842